

SAMSUNG

GSM TELEPHONE
SGH-X600

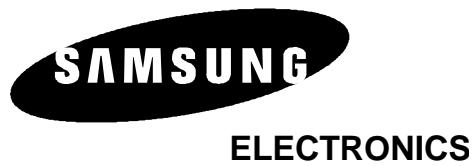
SERVICE *Manual*

GSM TELEPHONE

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BASIC.

1. SGH-X600 Specification

1. GSM General Specification

	GSM900 Phase 1	EGSM 900 Phase 2	DCS1800 Phase 1
Freq. Band[MHz] Uplink/Downlink	890~915 935~960	880~915 925~960	1710~1785 1805~1880
ARFCN range	1~124	0~124 & 975~1023	512~885
Tx/Rx spacing	45MHz	45MHz	95MHz
Mod. Bit rate/ Bit Period	270.833kbps 3.692us	270.833kbps 3.692us	270.833kbps 3.692us
Time Slot Period/Frame Period	576.9us 4.615ms	576.9us 4.615ms	576.9us 4.615ms
Modulation	0.3GMSK	0.3GMSK	0.3GMSK
MS Power	33dBm~13dBm	33dBm~5dBm	30dBm~0dBm
Power Class	5pcl ~ 15pcl	5pcl ~ 19pcl	0pcl ~ 15pcl
Sensitivity	-102dBm	-102dBm	-100dBm
TDMA Mux	8	8	8
Cell Radius	35Km	35Km	2Km

2. GSM TX power class

TX Power control level	GSM900
5	33 ±2 dBm
6	31 ±2 dBm
7	29 ±2 dBm
8	27 ±2 dBm
9	25 ±2 dBm
10	23 ±2 dBm
11	21 ±2 dBm
12	19 ±2 dBm
13	17 ±2 dBm
14	15 ±2 dBm
15	13 ±2 dBm
16	11 ±3 dBm
17	9 ±3dBm
18	7 ±3 dBm
19	5 ±3 dBm

TX Power control level	DCS1800
0	30 ±3 dBm
1	28 ±3 dBm
2	26 ±3 dBm
3	24 ±3 dBm
4	22 ±3 dBm
5	20 ±3 dBm
6	18 ±3 dBm
7	16 ±3 dBm
8	14 ±3 dBm
9	12 ±4 dBm
10	10 ±4 dBm
11	8 ±4dBm
12	6 ±4 dBm
13	4 ±4 dBm
14	2 ±5 dBm
15	0 ±5 dBm

2. SGH-X600 Circuit Description

1. SGH-X600 RF Circuit Description

1) RX PART

1. ASM(U102) Switching Tx, Rx path for GSM900, DCS1800 by logic controlling.

2. ASM Control Logic (Q100, Q101) Truth Table

	VC_1	VC_2
GSM Tx Mode	H	L
DCS Tx Mode	L	H
GSM Rx Mode	L	L
DCS Rx Mode	L	L

3. FILTER

To convert Electromagnetic Field Wave to Acoustic Wave and then pass the specific frequency band.

- GSM FILTER (F101) For filtering the frequency band between 925 ~ 960 MHz
- DCS FILTER (F102) For filtering the frequency band 1805 ~ 1880 MHz.

4. VC-TCXO (OSC101)

To generate the 26MHz reference clock to drive the logic and RF.

After additional process, the reference clock applies to the U103 Rx IQ demodulator and Tx IQ modulator.

The oscillator for RX IQ demodulator and Tx modulator are controlled by serial data to select channel and use fast lock mode for GPRS high class operation.

5. Transceiver (U103)

The receiver front-end converts the aerial RF signal from EGSM, DCS bands down to a low intermediate frequency (IF) of 100 kHz. The first stages are symmetrical low noise amplifiers (LNAs). They are matched to 50 ohm. The LNAs are followed by an I,Q down mixer. It consists of two mixers in parallel but driven by quadrature out of phase LO signals. The In phase (I) and quadrature phase (Q) IF signals are low pass filtered to provide protection from high frequency offset interferers. The low IF I and Q signals are then fed into the channel filter. The front-end low IF I and Q outputs enter the integrated bandpass channel filter with provision for five 8dB gain steps in front of the filters.

2) TX PART

Baseband IQ signal fed into offset PLL, this function is included inside of U103 chip.

OSC100 chip generates modulator signal which power level is about 6.5dBm and fed into Power Amplifier(U101).

The PA output power and power ramping are well controlled by Auto Power Control circuit.

We use offset PLL below .

Modulation Spectrum	200kHz offset 30 kHz bandwidth	GSM	-35dBc
		DCS	-35dBc
		PCS	-35dBc
	400kHz offset 30 kHz bandwidth	GSM	-66dBc
		DCS	-65dBc
		PCS	-66dBc
	600kHz ~ 1.8MHz offset 30 kHz bandwidth	GSM	-75dBc
		DCS	-68dBc
		PCS	-75dBc

2. Baseband Circuit description of SGH-X600

1. PCF50601

1.1. Power Management

Ten low-dropout regulators designed specifically for GSM applications power the terminal and help ensure optimal system performance and long battery life. A programmable boost converter provides support for 1.8V, 3.0V, and 5.0V SIMs, while a self-resetting, electronically fused switch supplies power to external accessories. Ancillary support functions, such as RTC module and High Voltage Charge pump, Clock generator, aid in reducing both board area and system complexity. I2C BUS serial interface provides access to control and configuration registers. This interface gives a microprocessor full control of the PCF50601 and enables system designers to maximize both standby and talk times.

Supervisory functions, including a reset generator, an input voltage monitor, and a temperature sensor, support reliable system design. These functions work together to ensure proper system behavior during start-up or in the event of a fault condition (low microprocessor voltage, insufficient battery energy, or excessive die temperature).

1.2. Backlight Brightness Modulator

The Backlight Brightness Modulator (BBM) contains a programmable Pulse-width modulator (PWM) and FET to modulate the intensity of a series of LED's or to control a DC/DC converter that drives LCD backlight.

This phone (SGH-X600) is not use PWM, but use DC CONTROL (COLOR_LCD_BL)

So "COLOR_LCD_BL" voltage is high value, backlight brightness is bright and "COLOR_LCD_BL" voltage is low value, backlight is gloomy .

1.3. Clock Generator

The Clock Generator (CG) generates all clocks for internal and external usage. The 32768 Hz crystal oscillator provides an accurate low clock frequency for the PCF50601 and other circuitry.

2. SGH-X600 Circuit Description

2. Connector

2-1. LCD Connector

LCD is consisted of LCD(color 65K STN LCD). Chip select signals in the U500, LCD_CS can enable LCD. This signal is from IO part of the DSP in the U500(alpha chip). "RESET_2.8V" signal initiates the Reset process of the LCD. 16-bit data lines(LD(0)~LD(15)) transfers data and commands to LCD through by pass capacitor. Data and commands use "RS" signal. If this signal is high, Inputs to LCD are commands. If it is low, Inputs to LCD are data. The signal which informs the input or output state to LCD, is required. But this system is not necessary this signal. So "L_WD" signal is used to write data or commands to LCD. Power signal for LCD is "VDD2".

2-2. IRDA

This system uses IRDA module, HSDL_3208, Agilent's. This has signals, "IRDA_DOWN"(enable signal), "RXD0"(input data) and "TXD0"(output data). These signals are connected to OM6357. It uses two power signals. "VDD2" is used for circuit and "VBAT" is used for LED.

2-3. Key

This is consisted of key interface pins among OM6357, KBIO(0:7). These signals compose the matrix. Result of matrix informs the key status to key interface in the OM6357. Power on/off key is separated from the matrix. So power on/off signal is connected with PCF50601 to enable PCF50601. Ten key LEDs use the "BLVDD" supply voltage. "COLOR_LCD_BL" signal enables LEDs with current control.

2-4. EMI ESD Filter

This system uses the EMI ESD filter, EMIF09 to protect noise from IF CONNECTOR part.

2-5 IF connetor

It is 18-pin connector. They are designed to use VBAT, V_EXT_CHARGE, TXD0, RXD0, RTS0, CTS0, JIG_REC, CHARGER_OK, RXD1, TXD1, AUX_MIC, AUX_SPK and GND. They connected to power supply IC, microprocessor and signal processor IC.

3. Battery Charge Management

A complete constant-current/constant-voltage linear charger for single cell lithium-ion batteries.

If ta connected to phone, "V_EXT_CHARGE" enable charger IC and supply current to battery.

When fault condition caused, "CHG_ON" signal level change low to high and charger IC stop charging process.

4. Audio

EARP_P and EARP_N from OM6357 are connected to the main receiver. AUXSP is connected to the Hands free kit. MIC_P and MIC_N are connected to the main MIC. And AUX_MIC_P and AUX_MIC_N are connected to the Hands free kit.

YMU762C is a LSI for portable telephone that is capable of playing high quality music by utilizing FM synthesizer and ADPCM decoder that are included in this device.

As a synthesis, YMU762C is equipped 32 voices with different tones. Since the device is capable of simultaneously generating up to synchronous with the play of the FM synthesizer, various sampled voices can be used as sound effects.

Since the play data of YMU762C are interpreted at anytime through FIFO, the length of the data(playing period) is not limited, so the device can flexibly support application such as incoming call melody music distribution service.

The hardware sequencer built in this device allows playing of the complex music without giving excessive load to the CPU of the portable telephones. Moreover, the registers of the FM synthesizer can be operated directly for real time sound generation, allowing, for example, utilization of various sound effects when using the game software installed in the portable telephone.

YMU762C includes a speaker amplifier with high ripple removal rate whose maximum output is 550mW (SPVDD=3.6V). The device is also equipped with conventional function including a vibrator and a circuit for controlling LEDs synchronous with music.

For the headphone, it is provided with a stereophonic output terminal.

For the purpose of enabling YMU762C to demonstrate its full capabilities, Yamaha purpose to use "SMAF:Synthetic music Mobile Application Format" as a data distribution format that is compatible with multimedia. Since the SMAF takes a structure that sets importance on the synchronization between sound and images, various contents can be written into it including incoming call melody with words that can be used for training karaoke, and commercial channel that combines texts, images and sounds, and others. The hardware sequencer of YMU762C directly interprets and plays blocks relevant to synthesis (playing music and reproducing ADPCM with FM synthesizer) that are included in data distributed in SMAF.

5. Memory

signals in the OM6357 enable two memories. They use only one volt supply voltage, VDD3 in the PCF50601. This system uses Samsung's memory, KBB06A300M-T402. It is consisted of 128M bits flash NOR memory and 128M bits flash NAND memory and 32M bits UtRAM. It has 16 bit data line, HD[0~15] which is connected to OM6357 and MV317SA. It has 23 bit address lines, HA[1~23]. CS_NAND and NCSRAM signals is chip select. Writing process, HWR_N is low and it enables writing process to flash memory and SRAM. During reading process, HRD_N is low and it enables reading process to flash memory and SRAM. Each chip select signals in the OM6357 select memory among 2 flash memory and UtRAM. Reading or writing procedure is processed after HWR_N or HRD_N is enabled. Memories use reset, which is VDD3 delay from PCF50601. HA[22] signal enables lower byte of SRAM and HA[23] signal enables higher byte of SRAM.

6. OM6357

OM6357 is consisted of ARM core and DSP core. It has 8x1Kword on-chip program/data RAM, 55Kwords on-chip program ROM in the DSP. It has 4K*32bits ROM and 2K*32bits RAM in the ARM core. DSP is consisted of KBS, JTAG, EMI and UART. ARM core is consisted of EMI, PIC(Programmable Interrupt Controller), reset/power/clock unit, DMA controller, TIC(Test Interface Controller), PPI, SSI(Synchronous Serial Interface), ACC(Asynchronous communications controllers), timer, ADC, RTC(Real-Time Clock) and keyboard interface. KBIO(0:7), address lines of DSP core and HD[0~15]. HA[1~23], address lines of ARM core and HD[0~15], data lines of ARM core are connected to memory, YMU762C. MV317SA(Camera DSP Chip) controls the communication between ARM core and DSP core.

CS_NAND, NCSRAM, NCSFLASH in the ARM core are connected to each memory. HWR_N and HRD_N control the process of memory. External IRQ(Interrupt ReQuest) signals from each units, such as, PMU need the compatible process. KBIO[0~7] receive the status from key and RXD0/TXD0/irDA_DOWN are used for the communications using IRDA and data link cable(DEBUG_DTR/RTS/TXD/RXD/CTS/DSR).

It has JTAG control pins(TDI/TDO/TCK) for ARM core and DSP core. It receives 13MHz clock in CKI pin from external TCXO. ADC(Analog to Digital Converter) part receives the status of temperature, battery type and battery voltage.

2. SGH-X600 Circuit Description

7. TCO-9141G(26MHz)

This system uses the 26MHz TCXO, TCO-9141G, Toyocom. AFC control signal from OM6357 controls frequency from 26MHz x-tal. It generates the clock frequency. This clock is connected to OM6357, YMU762.

8. Camera DSP(MV317SA)

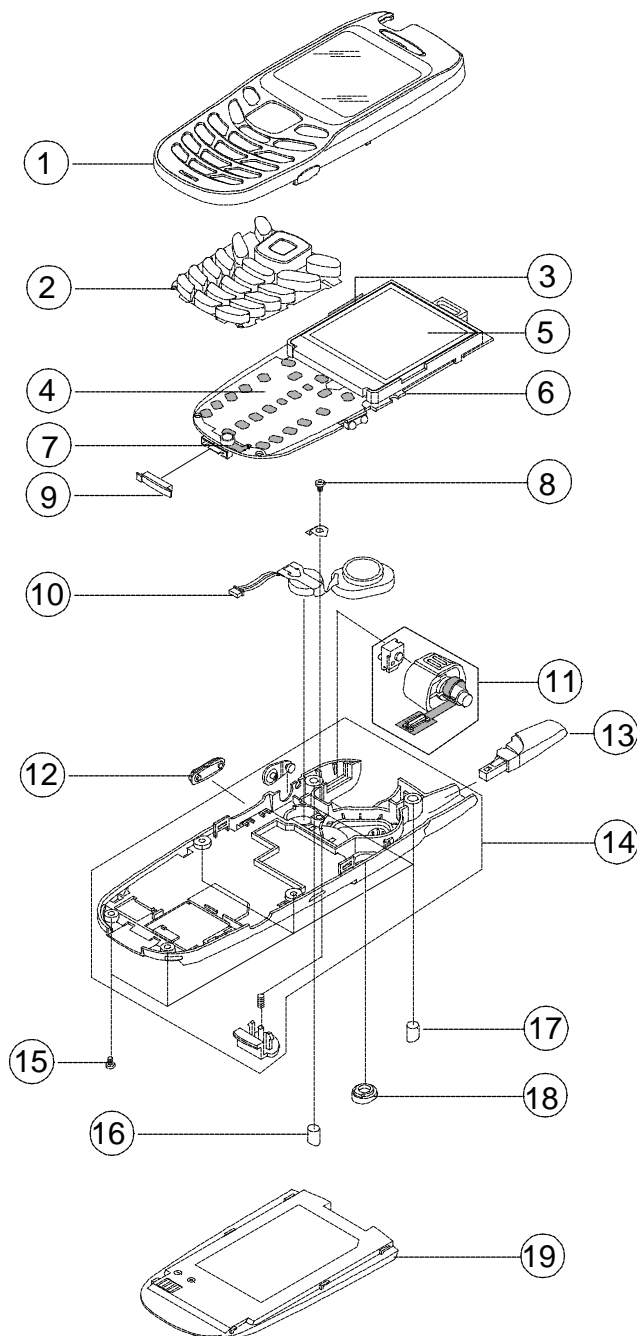
Tiger is an Integrated circuit for mobile phone camera. This structure will allow effectiveness for large data management and significantly reduces main processor will get burden.

In hence, Tiger will allow the user to be able to display to LCD direct without burdening the main processor. It also allows to have various kinds of display size on the LCD and snapshot for Jpeg. Digital effect will also be executed on real time base resulting Tiger as being a video co-processor in the mobile platform.

Also, an i80 type processor's 16bit parallel interface of Tiger makes it available for the CPU to interchange the data with Tiger. As the additional 8Mbit is usable except 2Mbit buffer embedded in Tiger, the diverse UI data processing which is not a burden to the CPU is available. JPEG encoder and decoder are baseline ISO/IEC 10918-1 JPEG compliance (DCT-based). JPEG decoder supports YUV444, YUV422, YUV420 and YUV411 format standard JPEG image.

3. SGH-X600 Exploded View and its Parts list

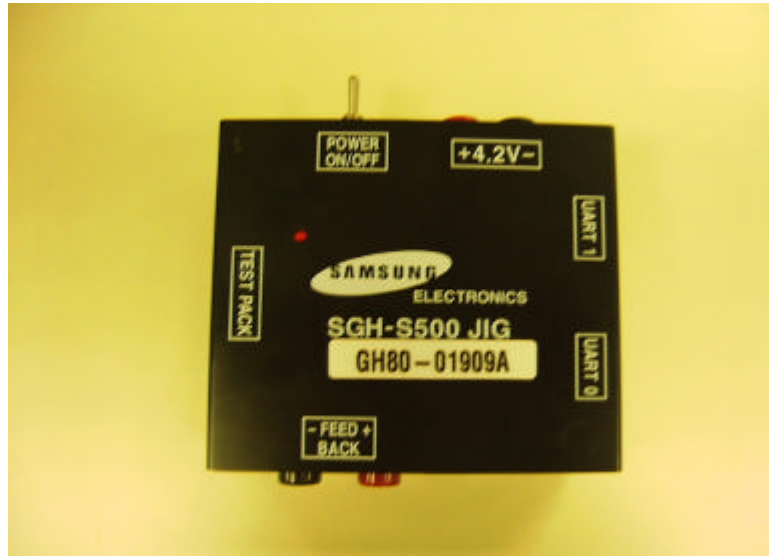
1. Cellular phone Exploded View



2. Cellular phone Parts list

N0	Description	SEC.CODE	REMARK
1	FRONT COVER	GH75-03273A	
2	KEYPAD	GH75-03274A	
3	VOLKEY FPCB	GH59-00953A	
4	DOME SHEET	GH59-00954A	
5	LCD	GH07-00421A	
6	MAIN PBA	GH92-01605A	
7	MIC	GH30-00057A	
8	SCREW	6001-001530	
9	IF COVER	GH73-02269A	
10	MOTOR_SPEAKER ASS'Y	GH59-01032A	
11	CAMERA	GH59-00969A	
12	VOLUME KEY	GH75-03275A	
13	ANTENNA	GH42-00354A	
14	REAR COVER	GH75-03276A	
15	SCREW	6001-001639	
16	SCREW CAP A	GH72-10691A	
17	SCREW CAP B	GH72-10692A	
18	RF COVER	GH72-10690A	
19	BATTERY	GH43-01033A	

3. Test Jig (GH80-01909A)



3-1. RF Test Cable
(GH39-00105A)



3-2. Test Cable
(GH39-00217A)



3-3. Serial Cable



3-4. Power Supply Cable



3-5. DATA CABLE
(GH39-00219A)



3-6. TA
(GH44-00482A)



4. SGH-X600 MAIN Electrical Parts List

SEC CODE	Design LOC	SEC CODE	Design LOC
0403-001387	ZD201	0801-002540	U202
0403-001446	D608	0801-002540	U205
0404-001172	D614	0801-002540	U300
0406-001083	D200	1001-001183	U201
0406-001083	D201	1003-001440	Q201
0406-001083	D300	1109-001280	U301
0406-001083	D601	1201-001954	U101
0504-001012	Q501	1202-001036	U204
0504-001012	Q502	1203-002633	U601
0504-001012	Q503	1203-002680	Q500
0504-001012	Q601	1203-002764	U203
0504-001151	Q100	1204-002161	U303
0504-001151	Q101	1205-002276	U200
0505-001423	Q300	1205-002327	U103
0506-000107	Q200	1205-002350	U400
0506-000107	Q600	1404-001221	TH201
0601-001611	D602	1405-001018	V502
0601-001611	D615	1405-001082	C200
0601-001790	D604	1405-001082	C221
0601-001790	D605	1405-001082	V201
0601-001790	D606	1405-001082	V202
0601-001790	D607	1405-001082	V203
0601-001790	D609	1405-001082	V204
0601-001790	D610	1405-001082	V205
0601-001790	D612	1405-001082	V300
0601-001790	D613	1405-001082	V301
0601-001823	D500	1405-001082	V302
0601-001823	D501	1405-001082	V303
0604-001261	D301	1405-001082	V503
0801-002237	U302	1405-001082	V505

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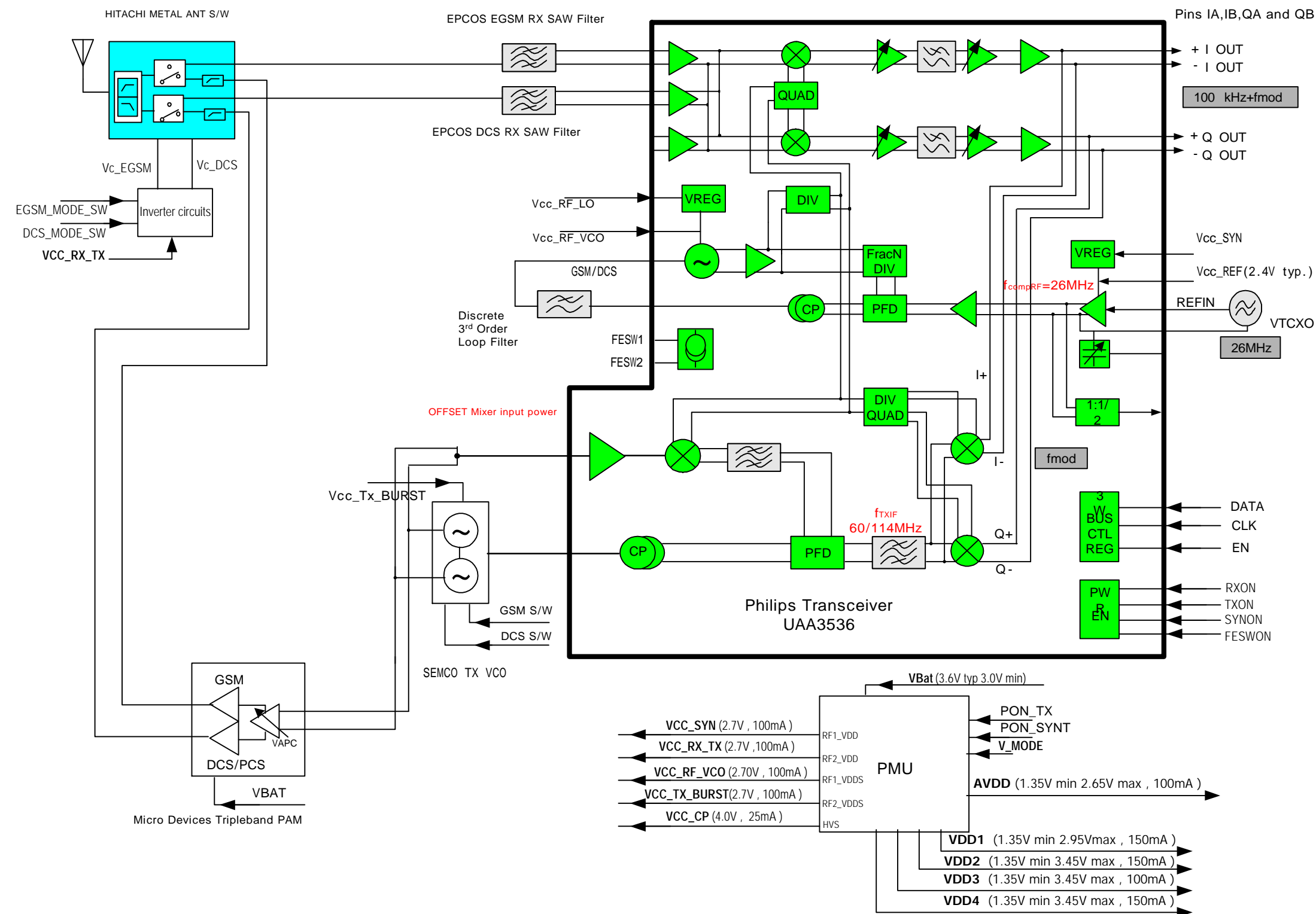
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2203-005482	C311
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2203-005482	C511
2203-005496	C132
2203-005496	C513
2203-005503	C134
2203-006053	C123
2203-005571	C428
2203-005571	C429
2203-006093	C502
2203-006093	C503
2203-006190	C137
2203-006190	C315
2203-006208	C253
2203-006208	C312

SEC CODE	Design LOC
2203-006208	C400
2203-006208	C404
2203-006208	C409
2203-006208	C417
2203-006208	C418
2203-006208	C421
2203-006208	C423
2203-006208	C430
2203-006208	C433
2203-006208	C438
2203-006208	C439
2301-001197	C122
2301-001213	C125
2404-001086	C609
2404-001105	C412
2404-001239	C126
2404-001268	C322
2404-001281	C422
2404-001281	C425
2703-001180	L103
2703-001722	L109
2703-001722	L113
2703-001723	L105
2703-001723	L107
2703-001723	L114
2703-001748	L108
2703-001748	L110
2703-001750	L102
2703-001750	L104
2703-002170	L100

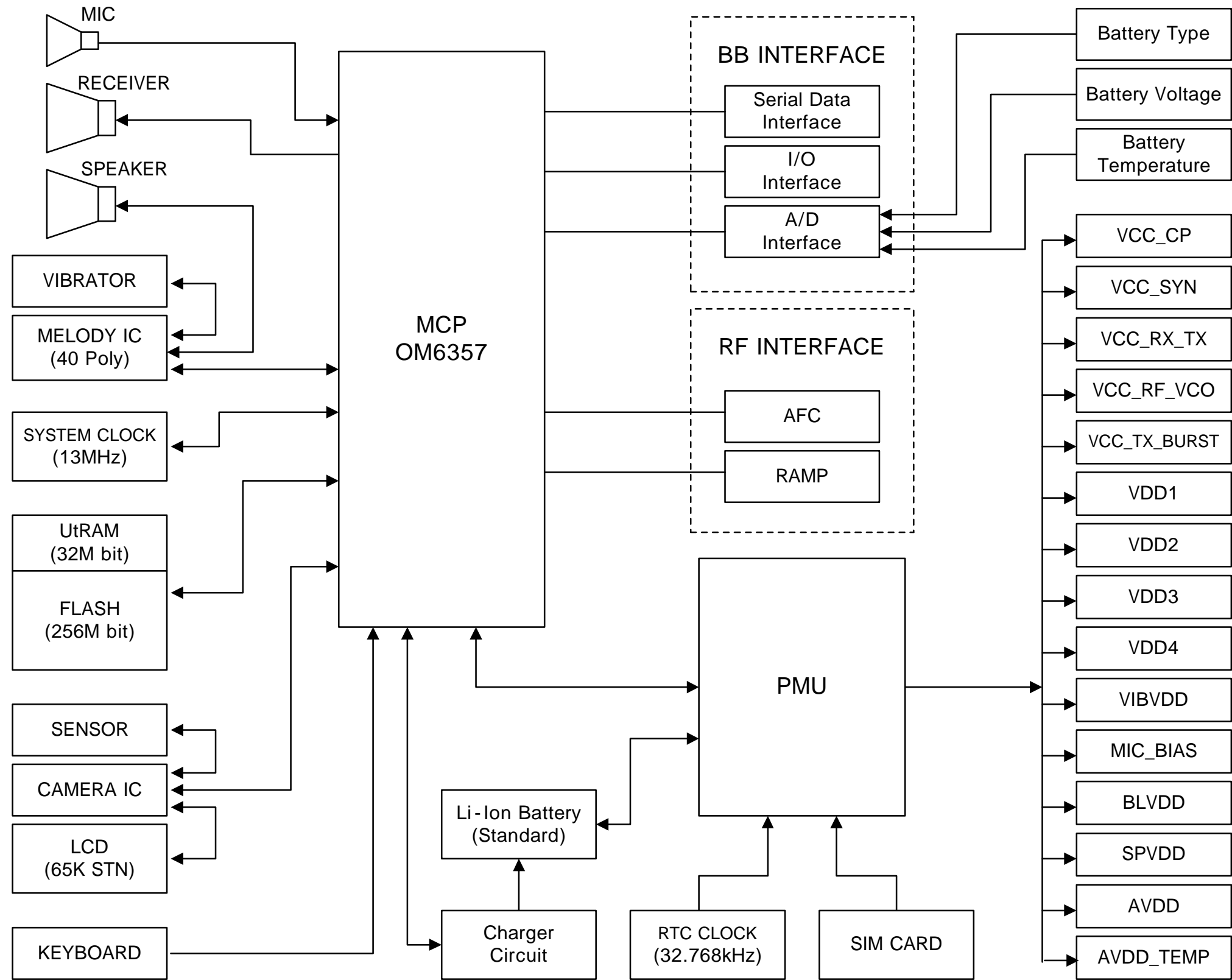
SEC CODE	Design LOC
2703-002199	L112
2703-002199	L115
2703-002203	L106
2703-002339	L600
2801-004025	X400
2801-004285	OSC500
2806-001326	OSC100
2809-001281	OSC101
2901-001246	U304
2904-001417	F101
2904-001419	F102
2909-001216	U102
3301-001105	L400
3705-001273	CN101
3709-001273	CN400
3710-001611	CN301
3711-005210	CN500
3711-005521	CN201
3711-005558	CN300
3722-001715	EAR201
4302-001130	BAT400
GH13-00019A	U500
GH71-02243A	ANT100

5. SGH-X600 Block Diagrams

1. RF Solution Block Diagram

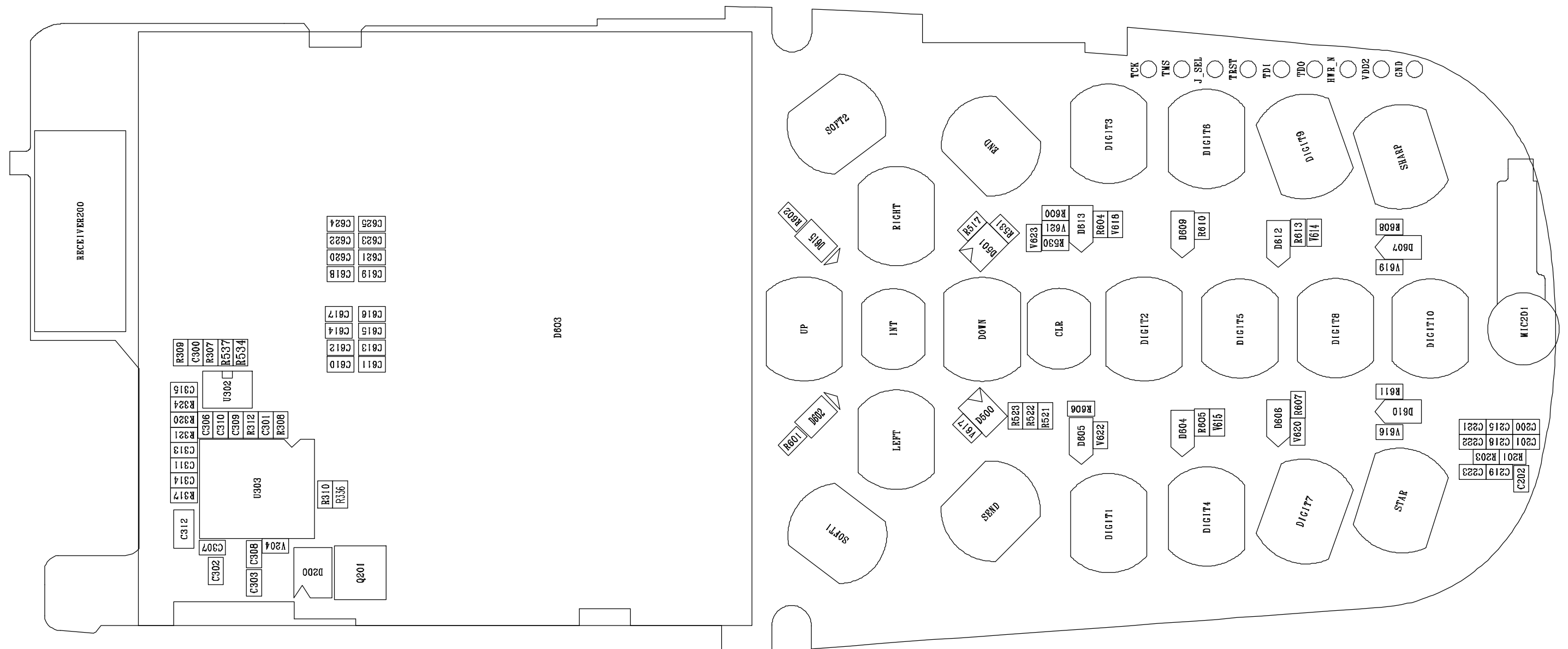


2. Base Band Solution Block Diagram

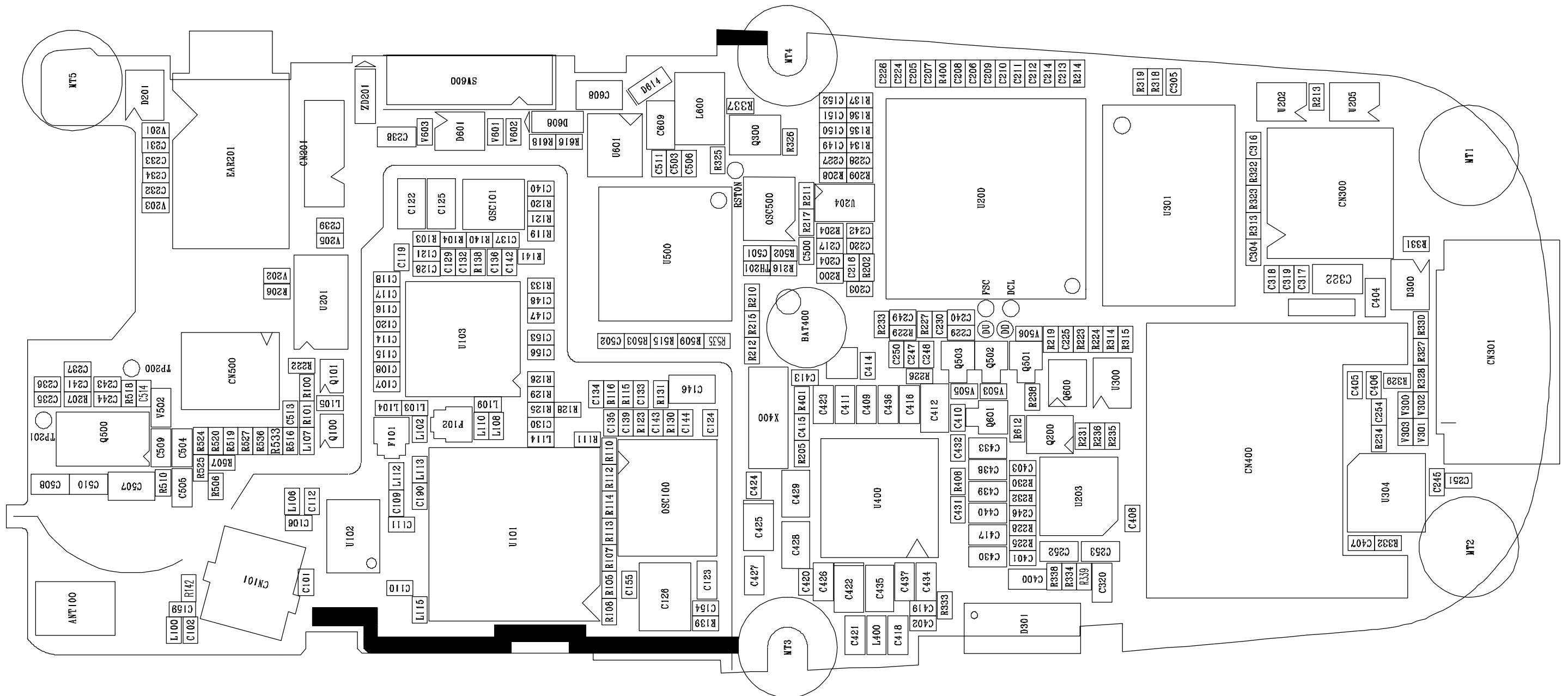


6. SGH-X600 PCB Diagrams

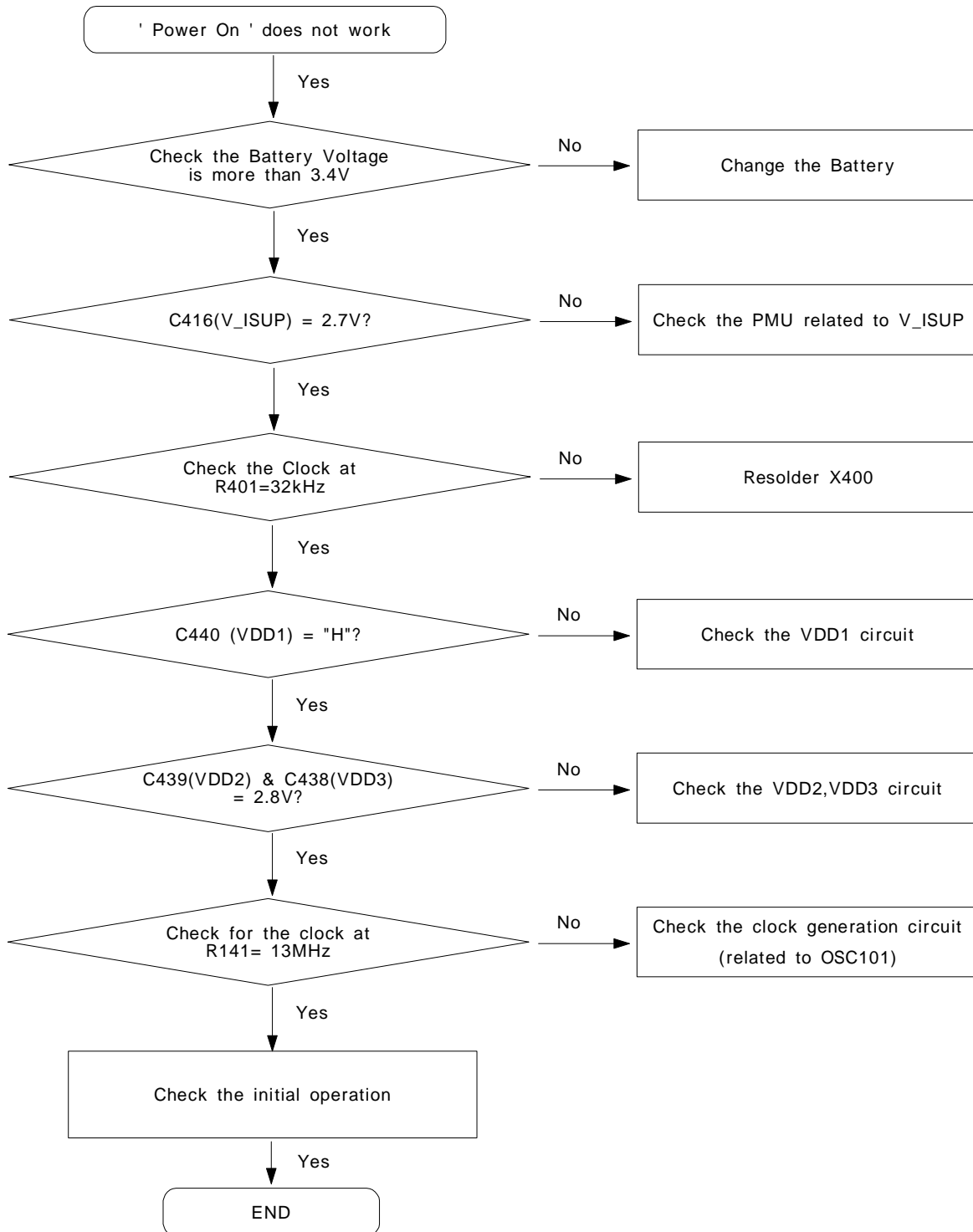
1. Main PCB Top Diagram



2. Main PCB Bottom Diagram

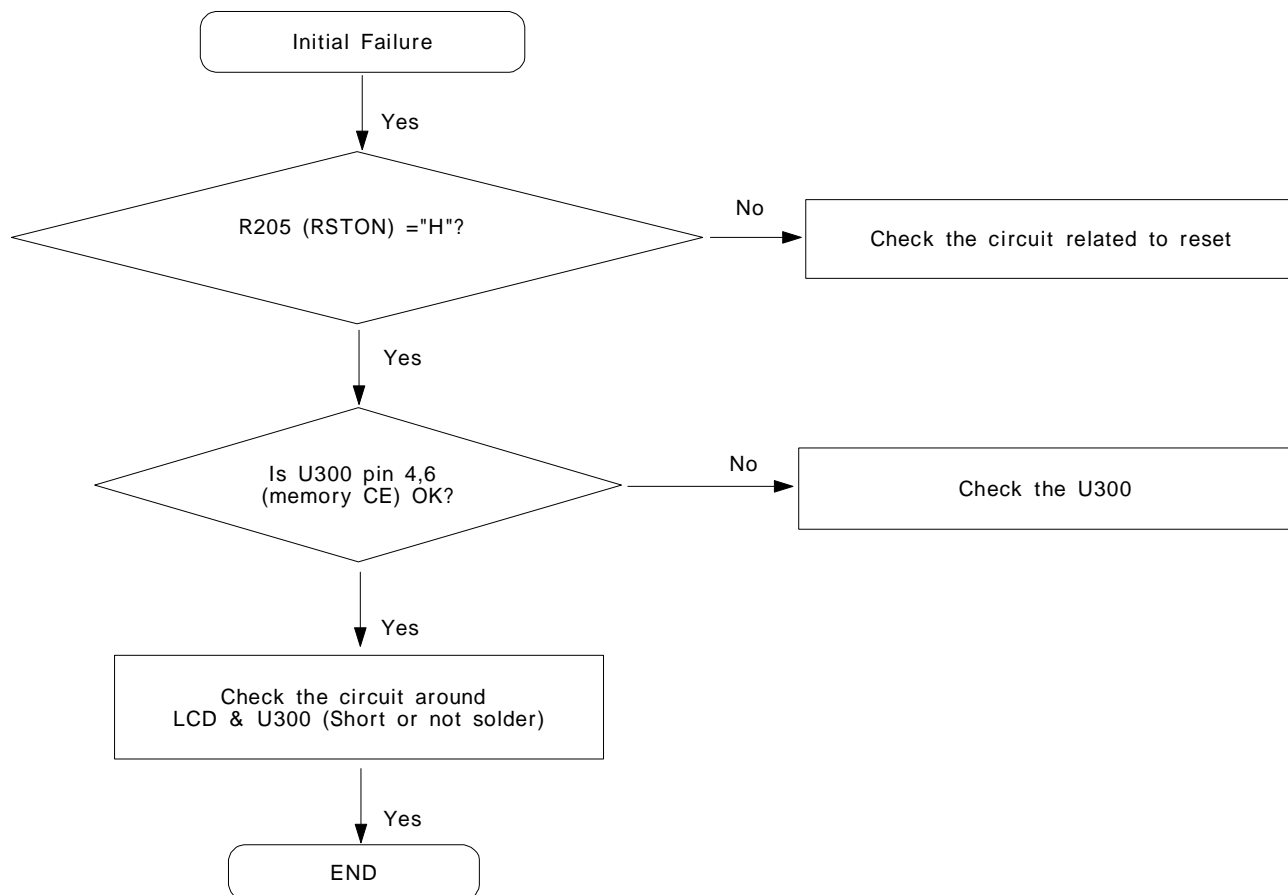


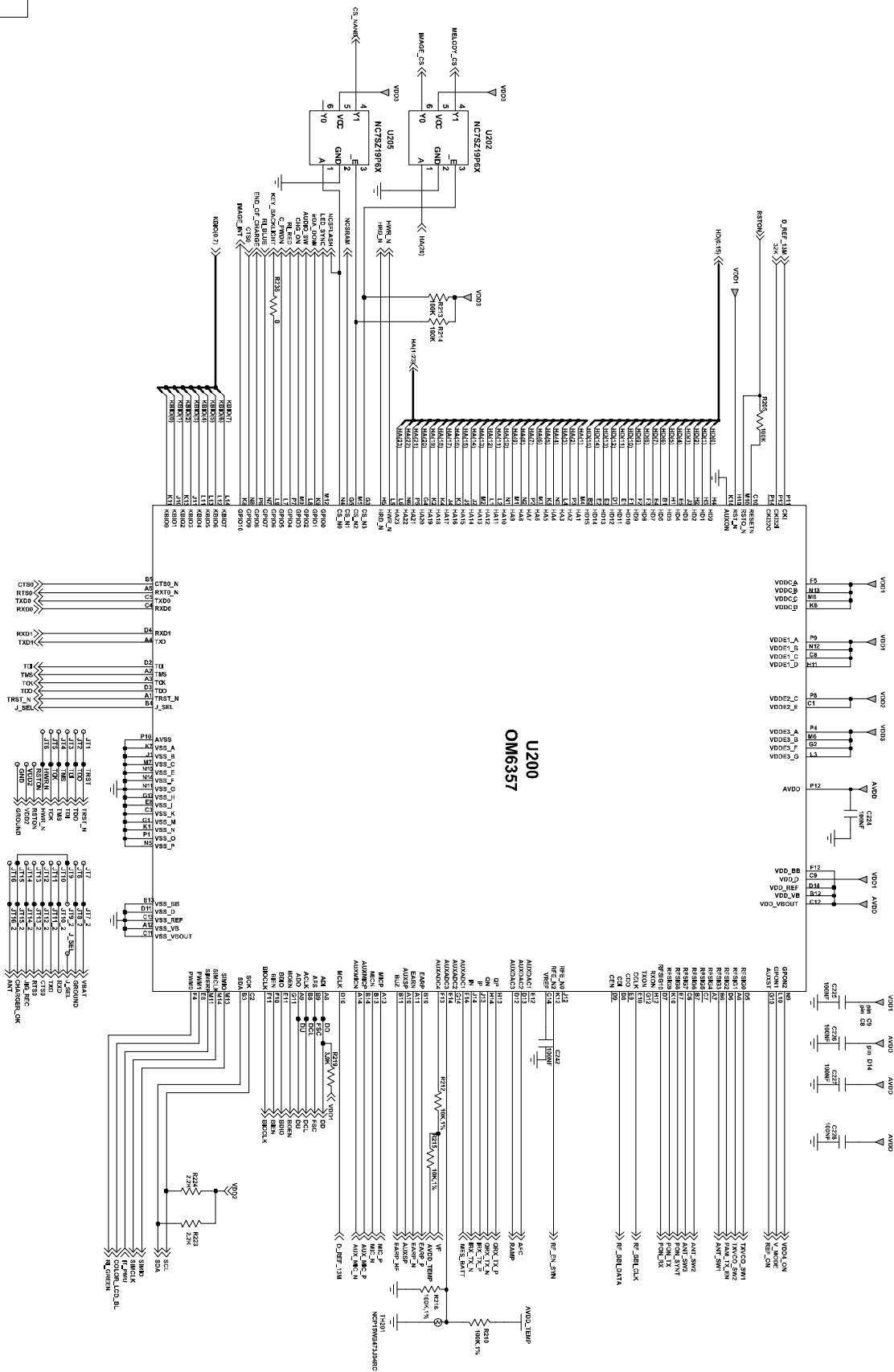
1. Power On



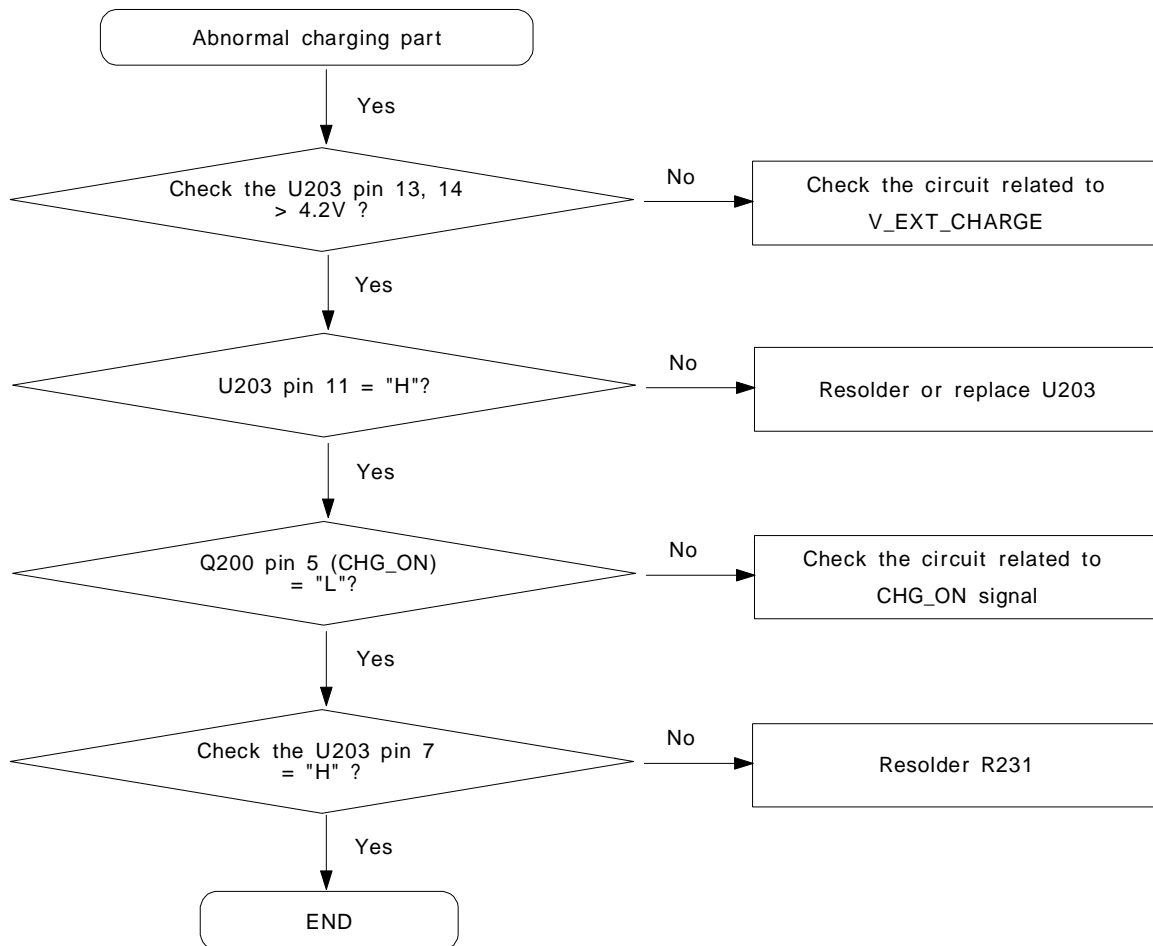


2. Initial

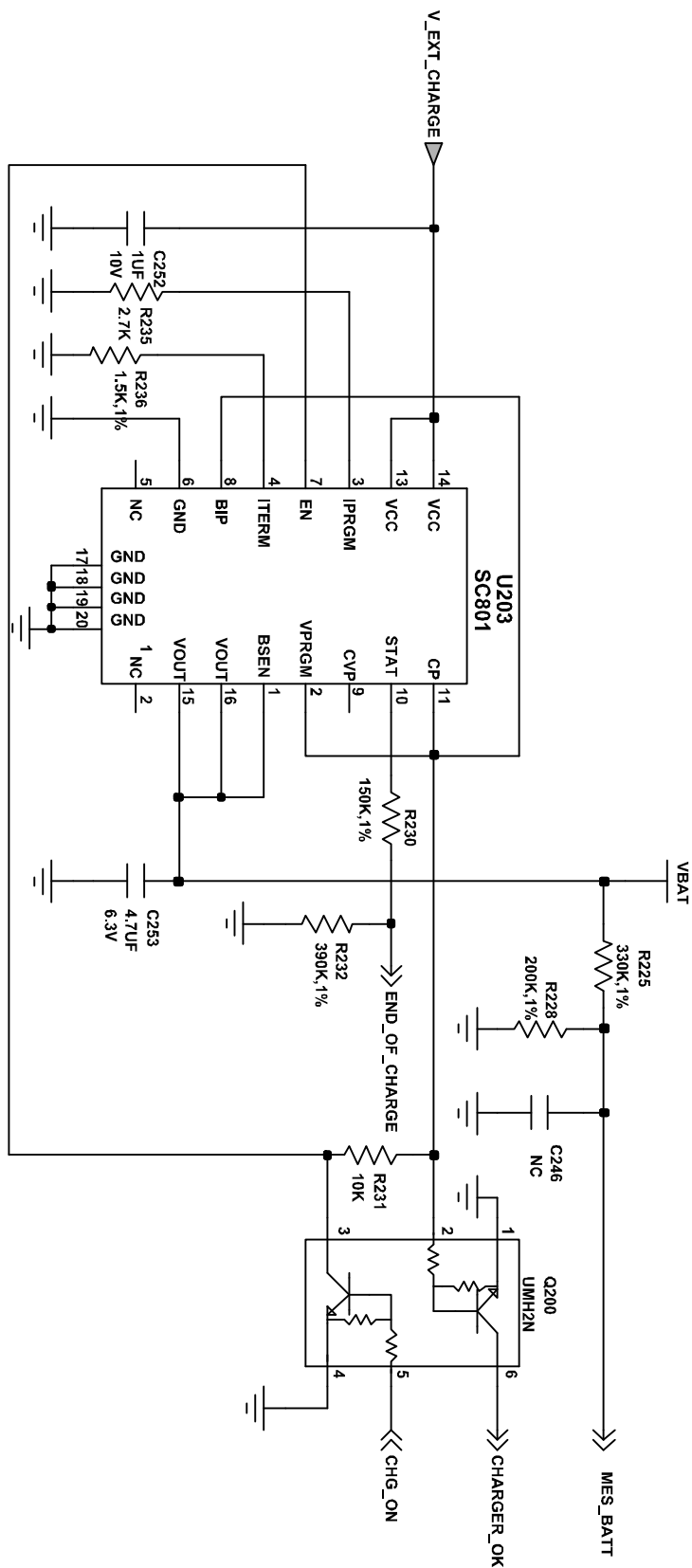




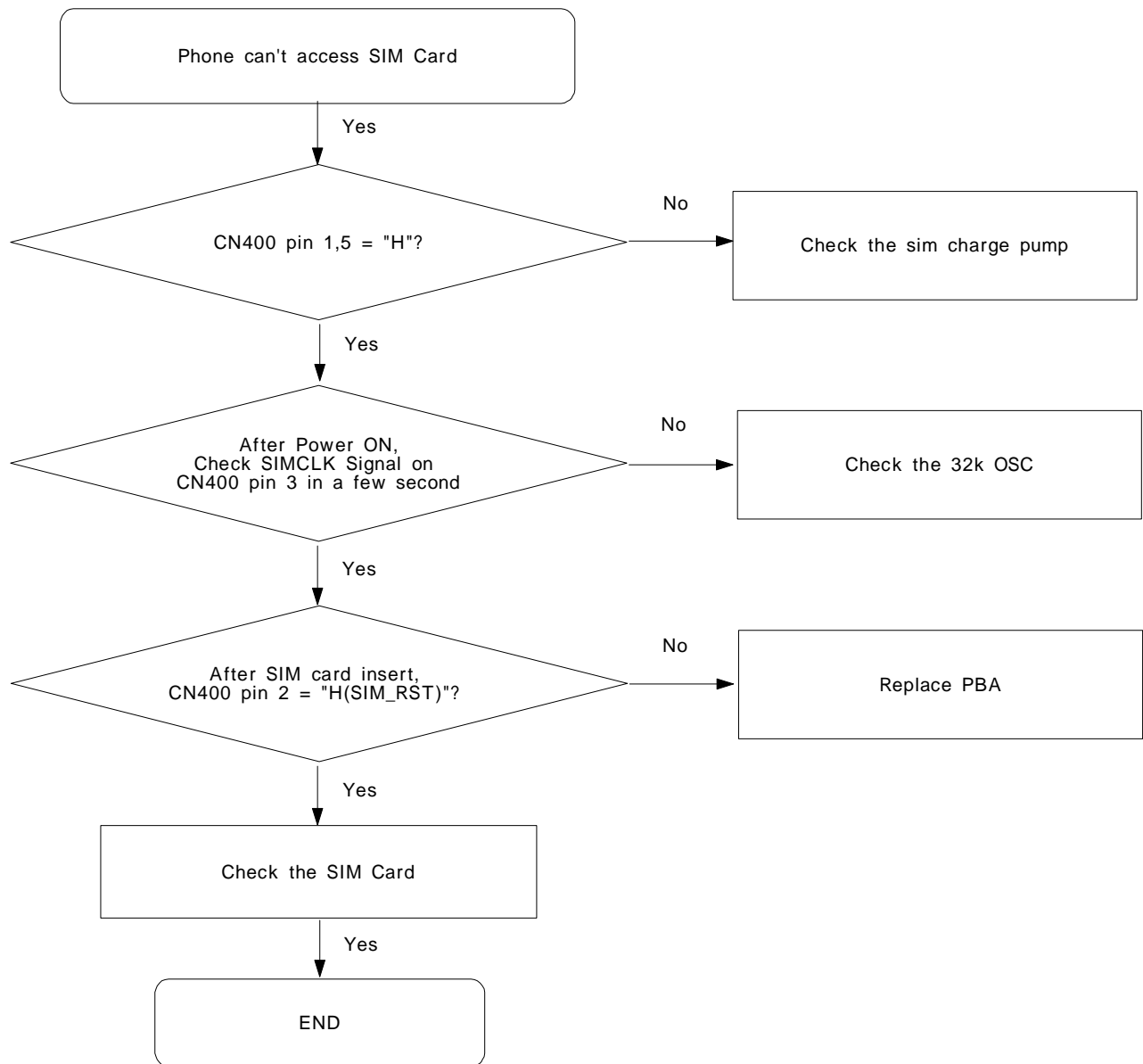
3. Charging Part



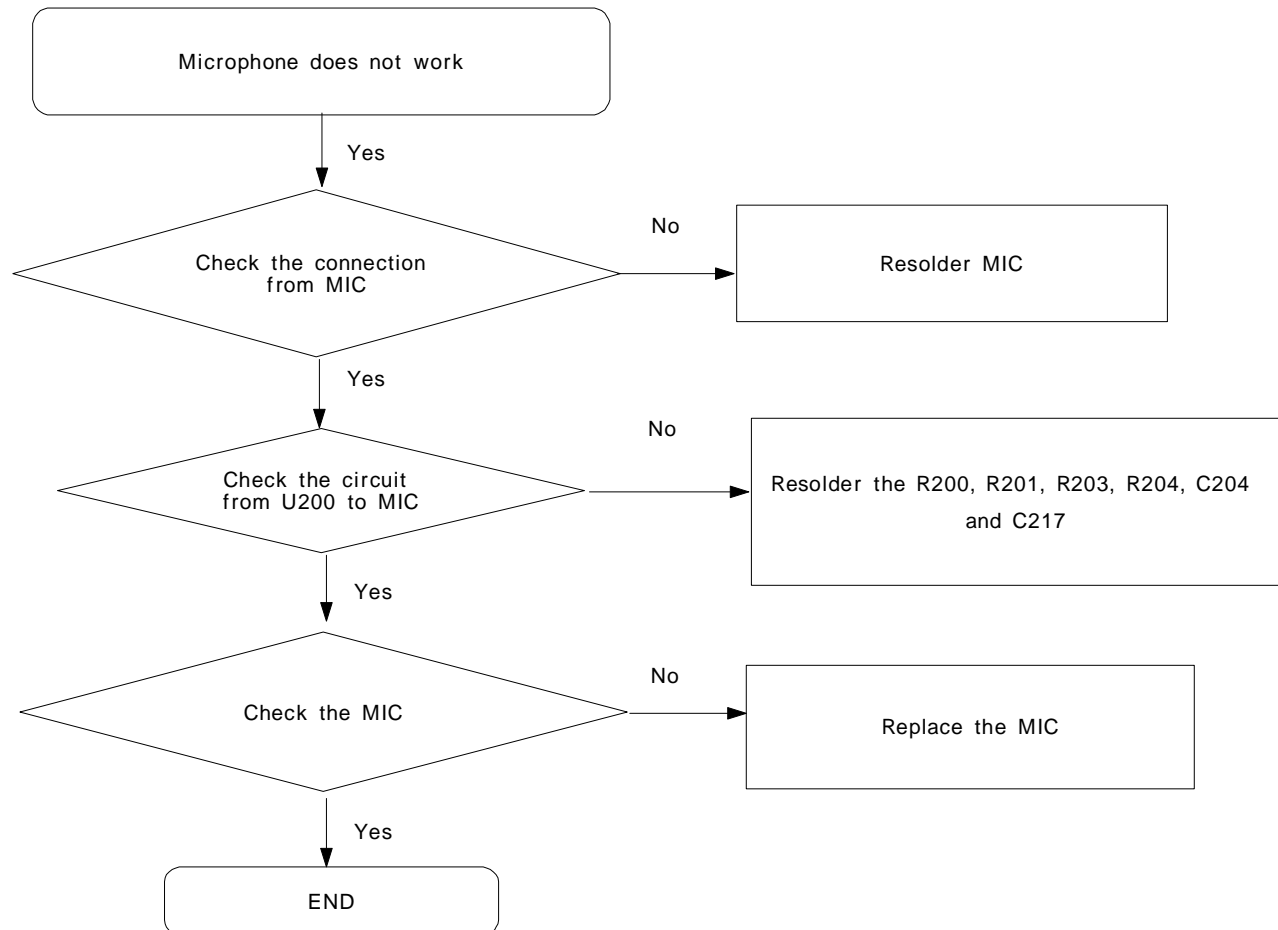
Charging



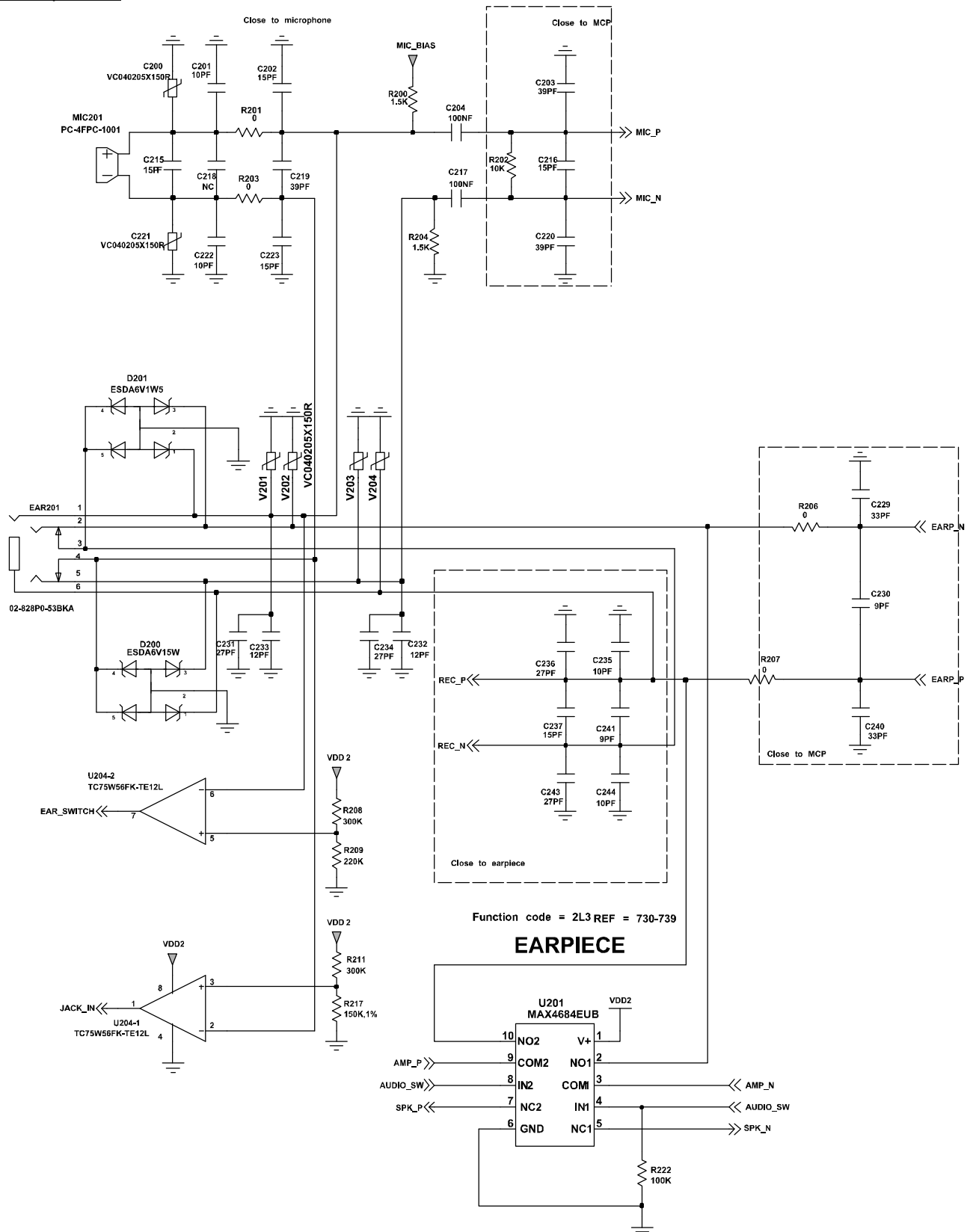
4. Sim Part



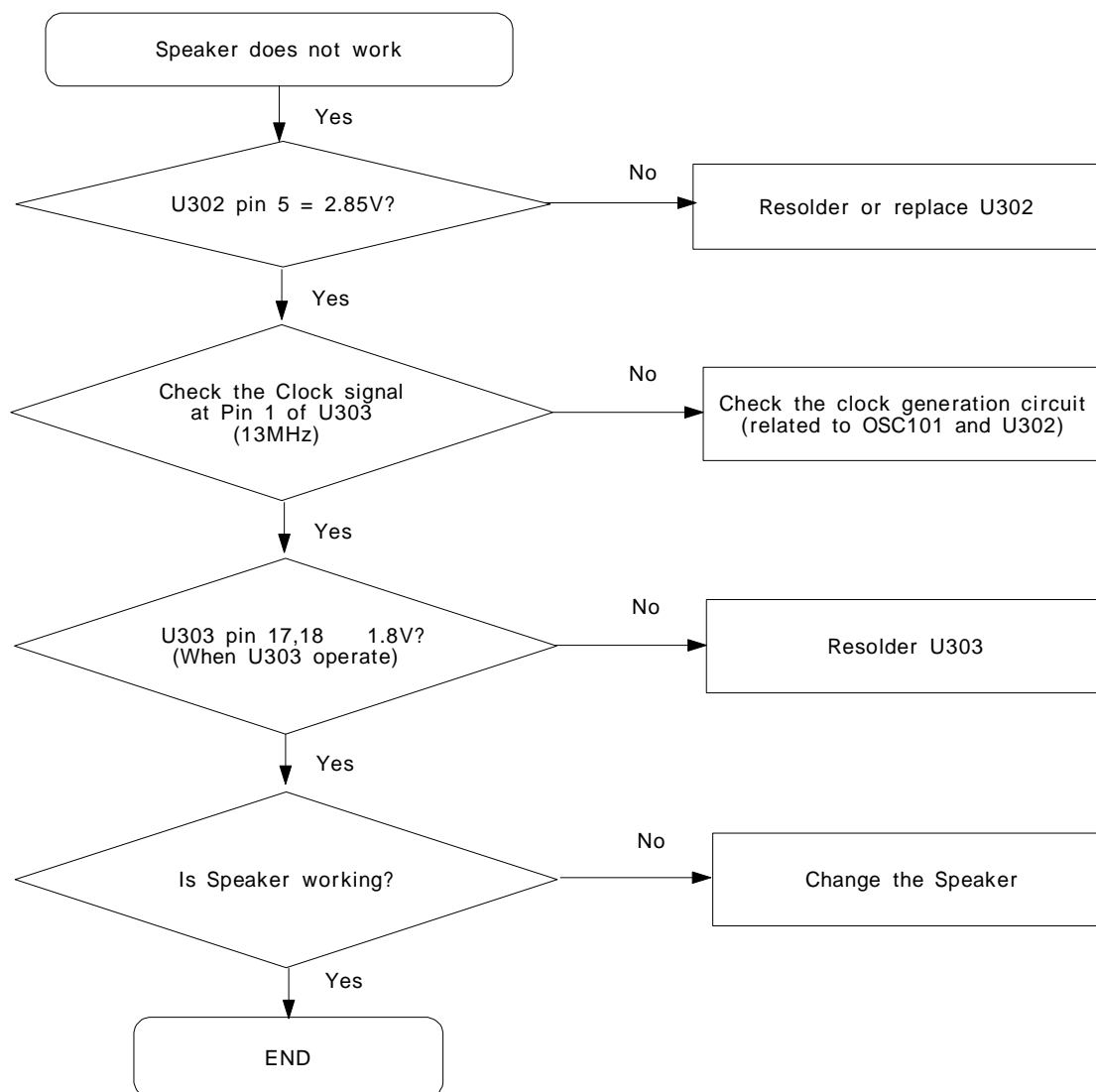
5. Microphone Part



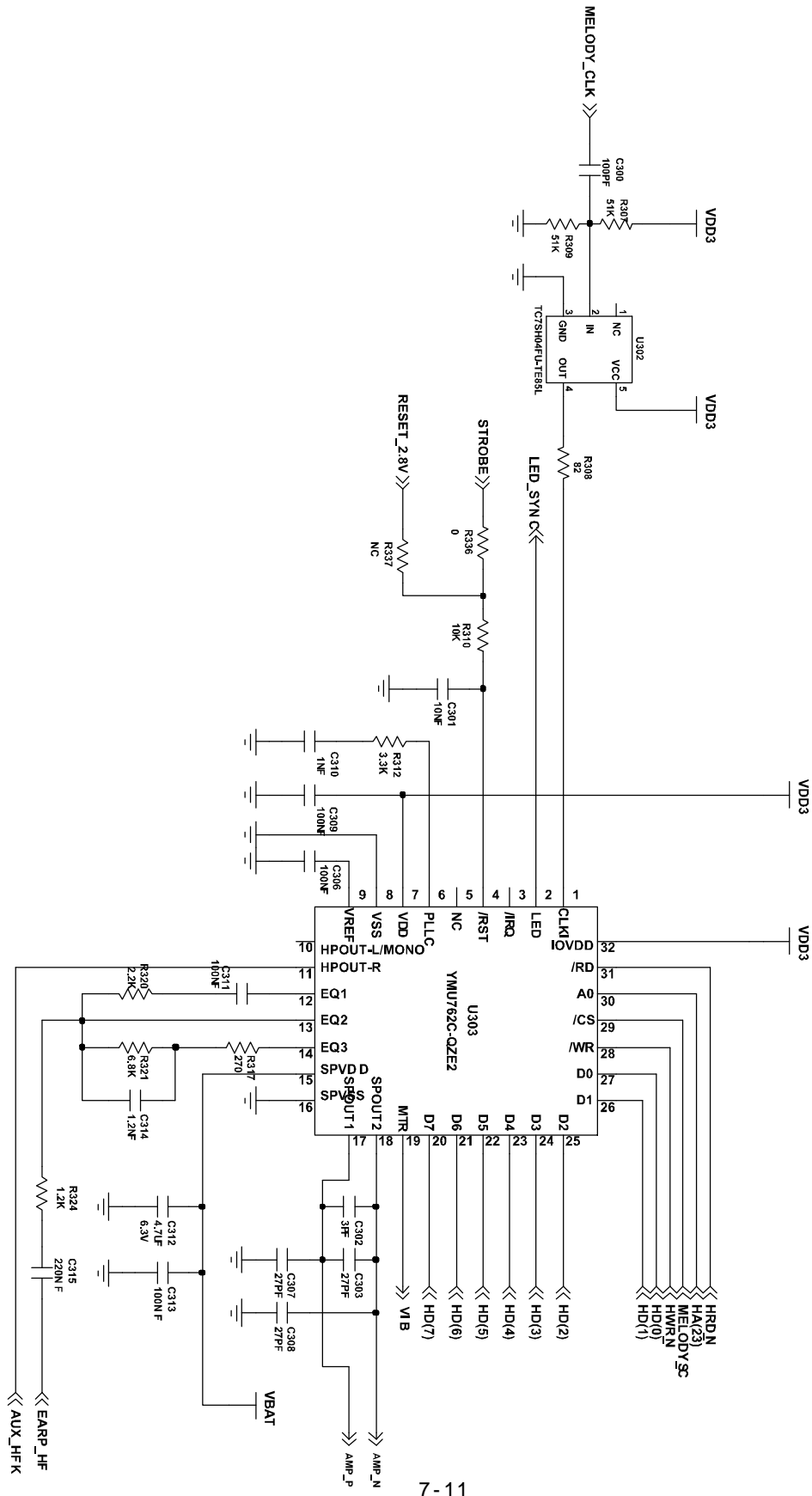
Microphone



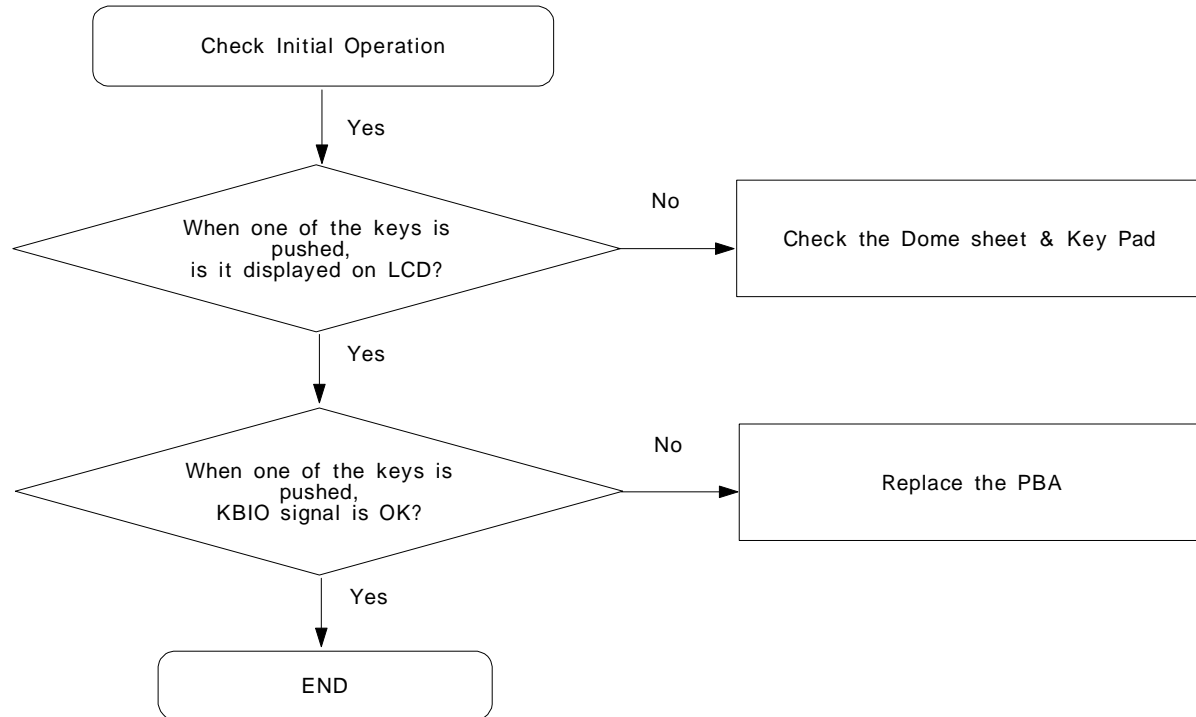
6. Speaker Part(Melody)



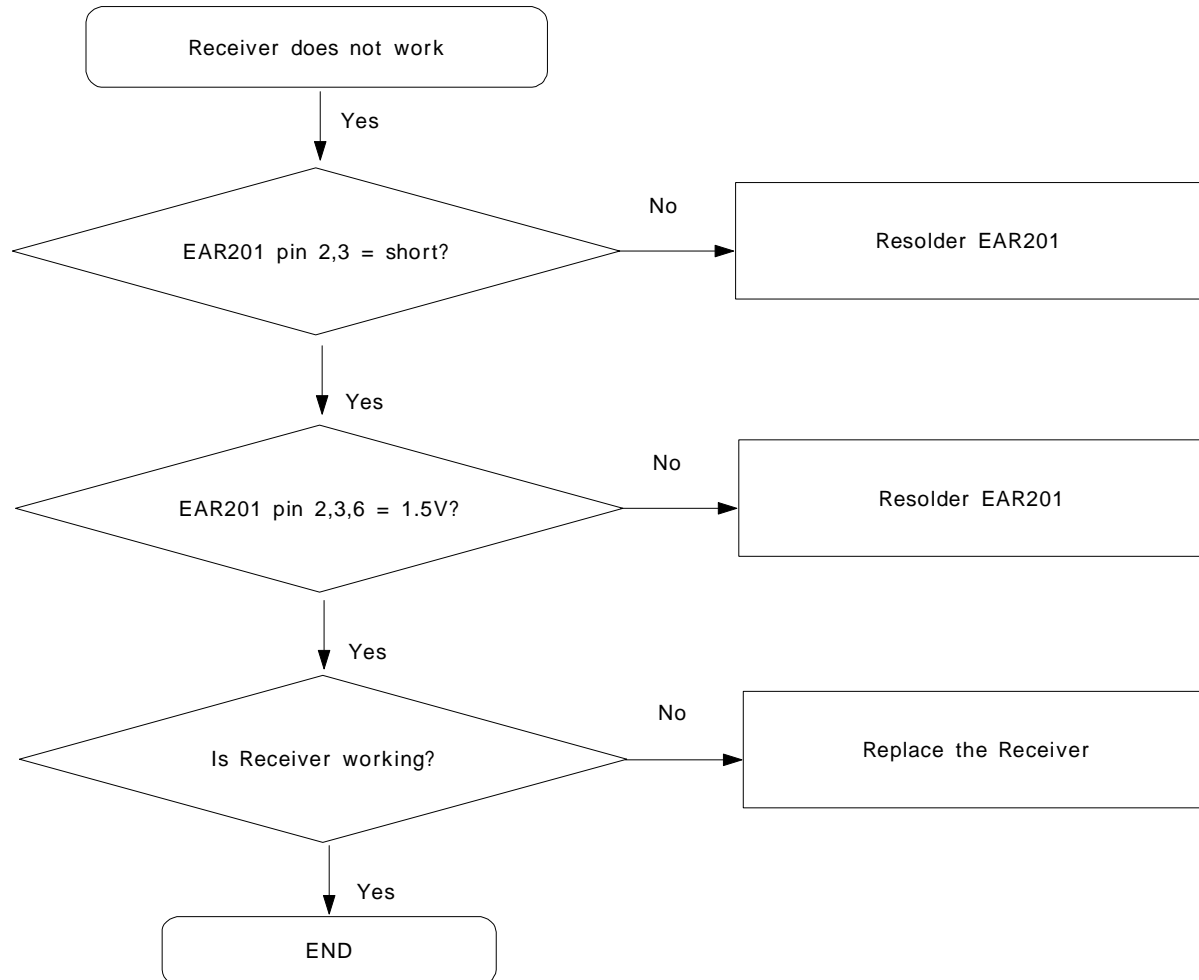
Speaker



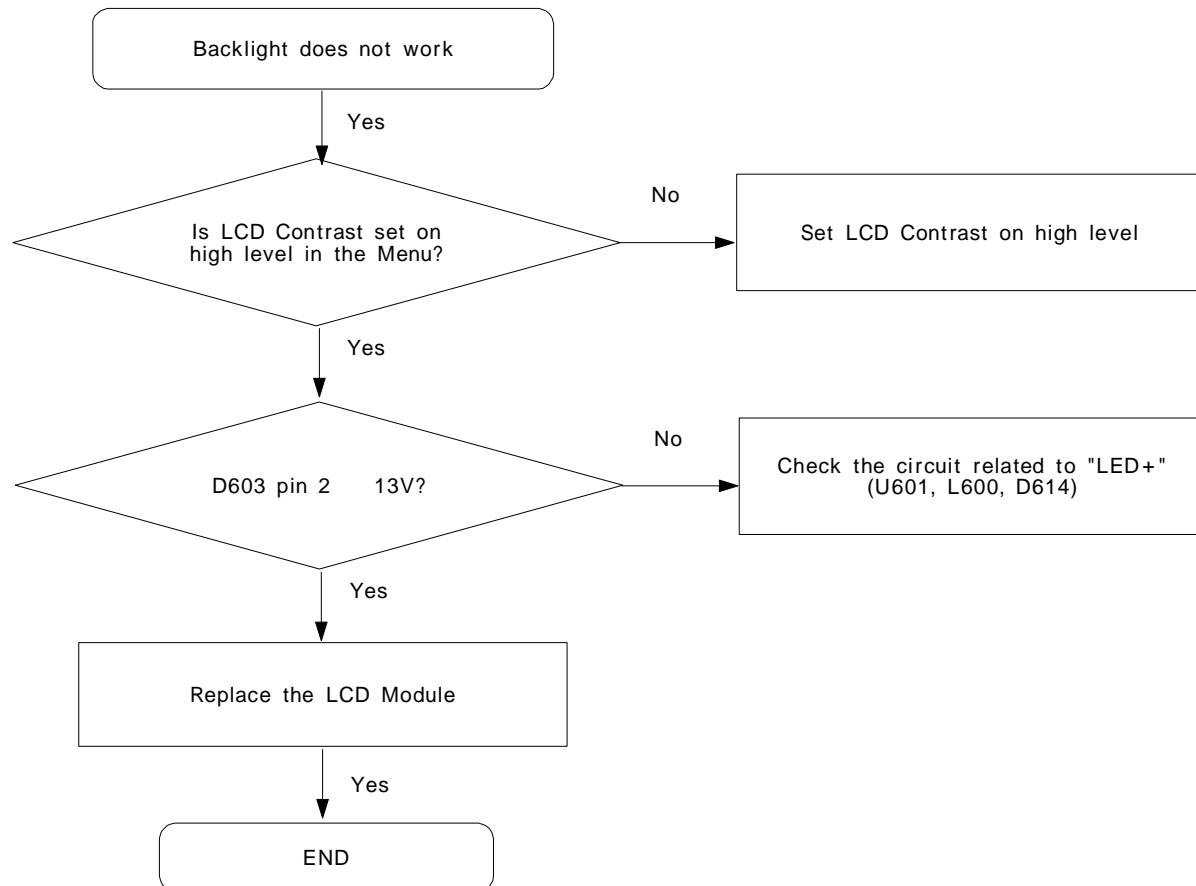
7. Key Data Input



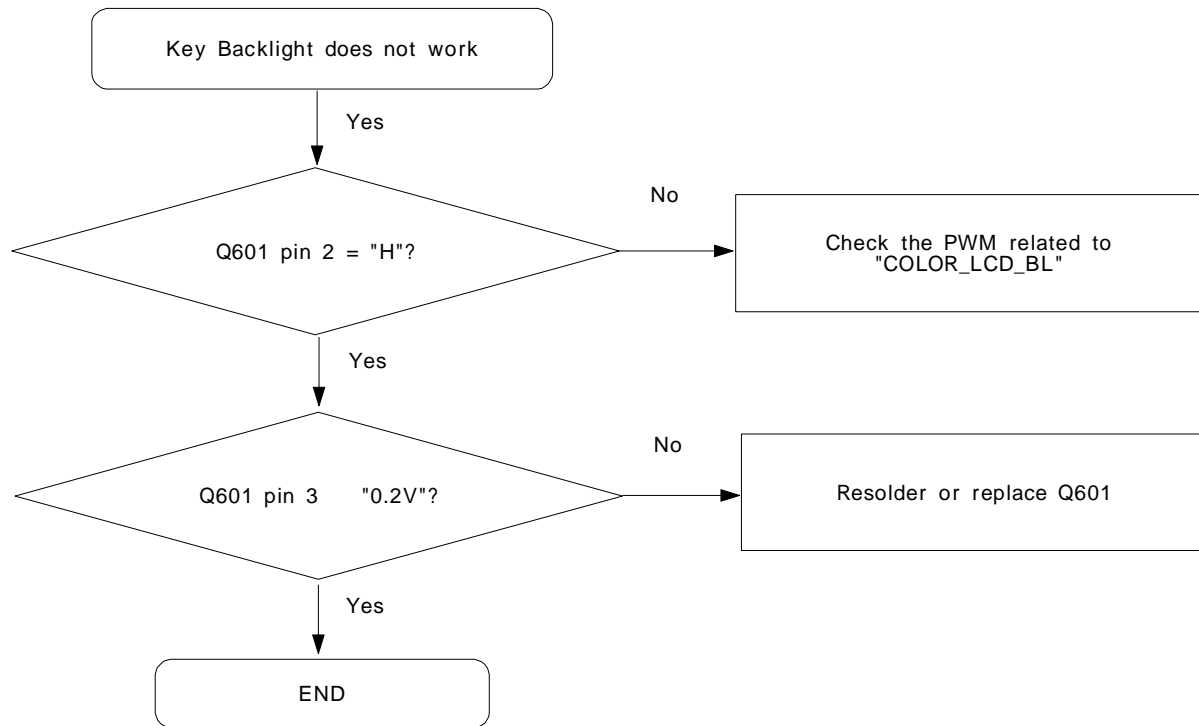
8. Receiver Part



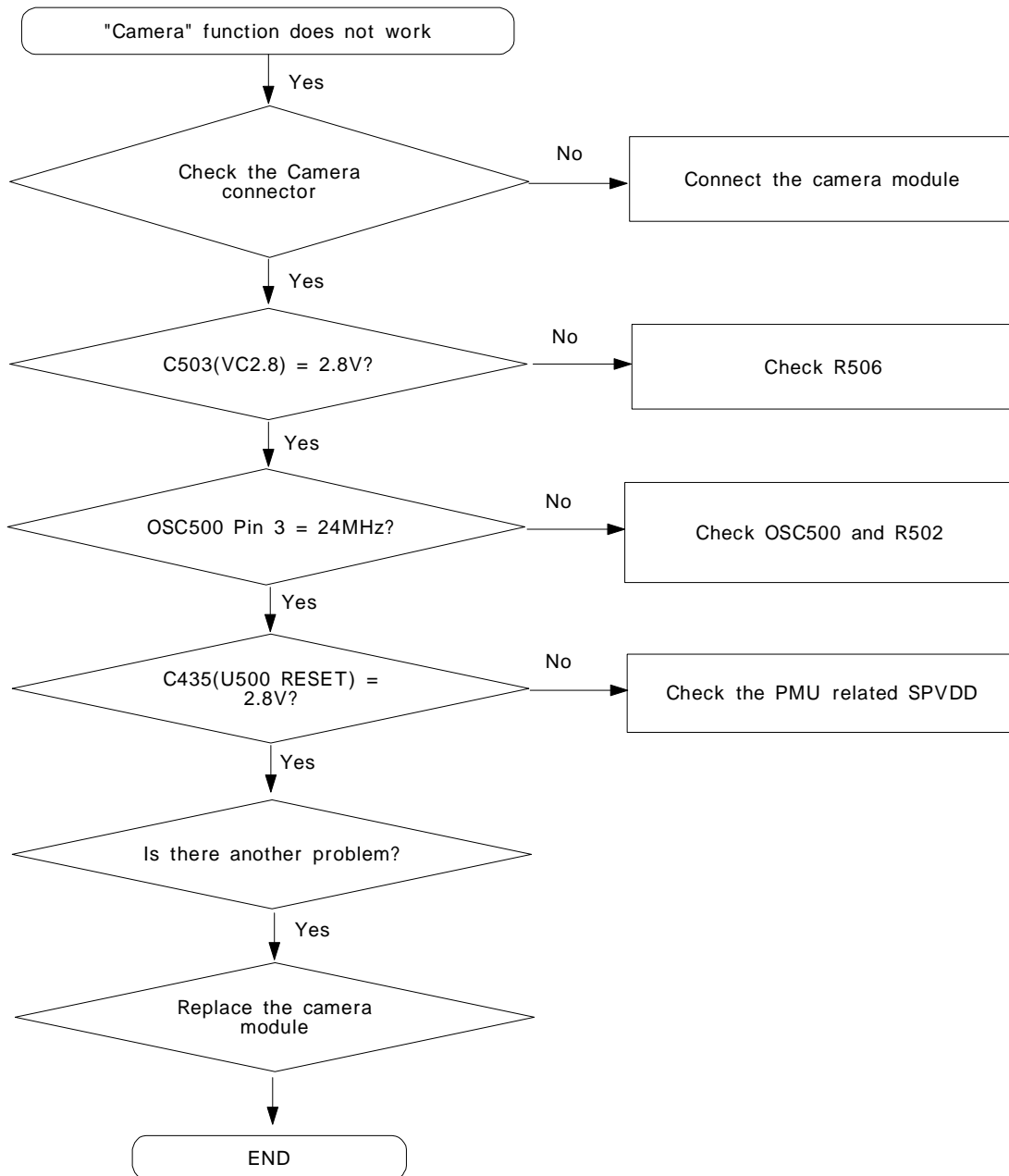
9. Back Light (for Color Main LCD)



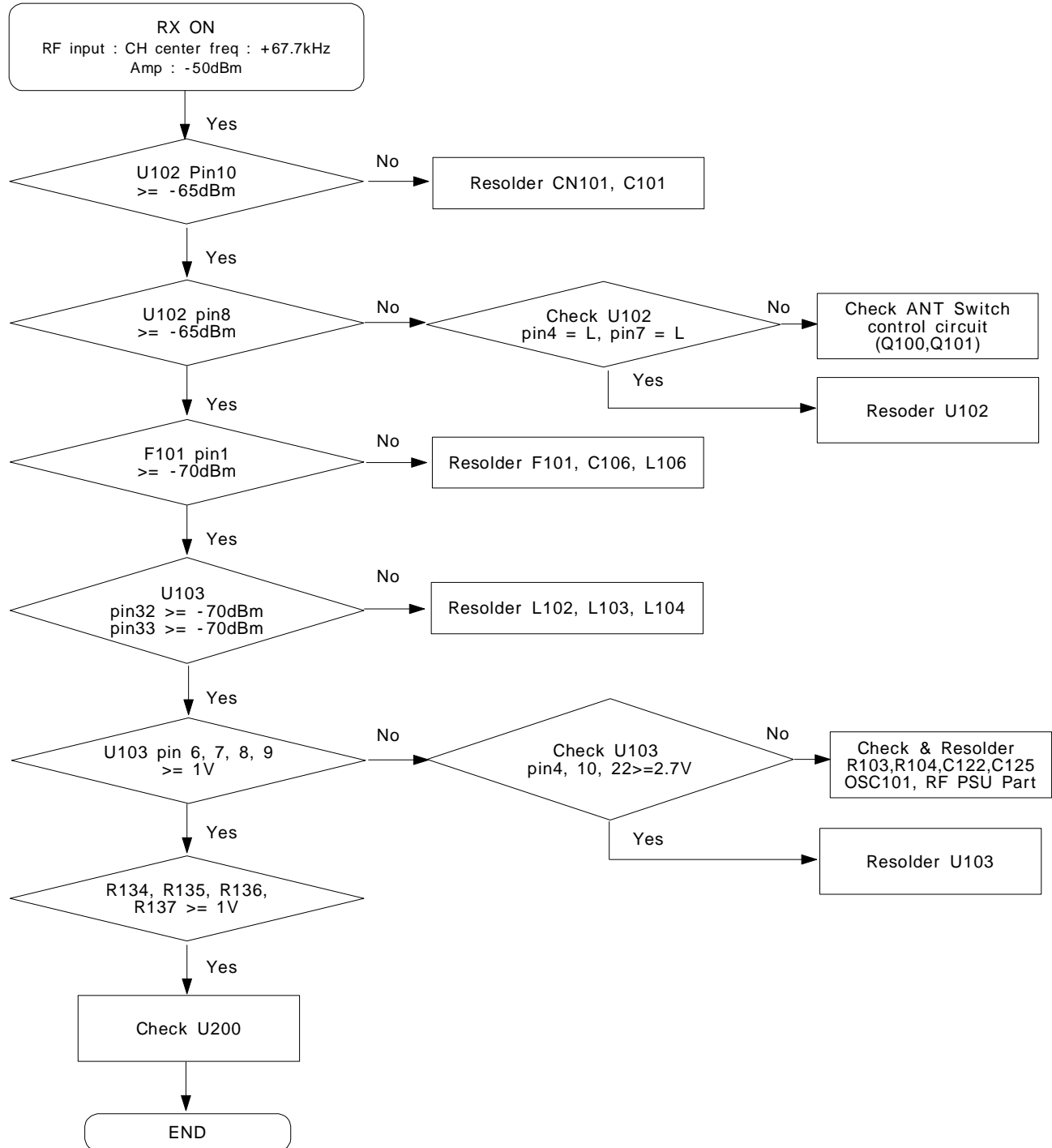
10. Key Back Light



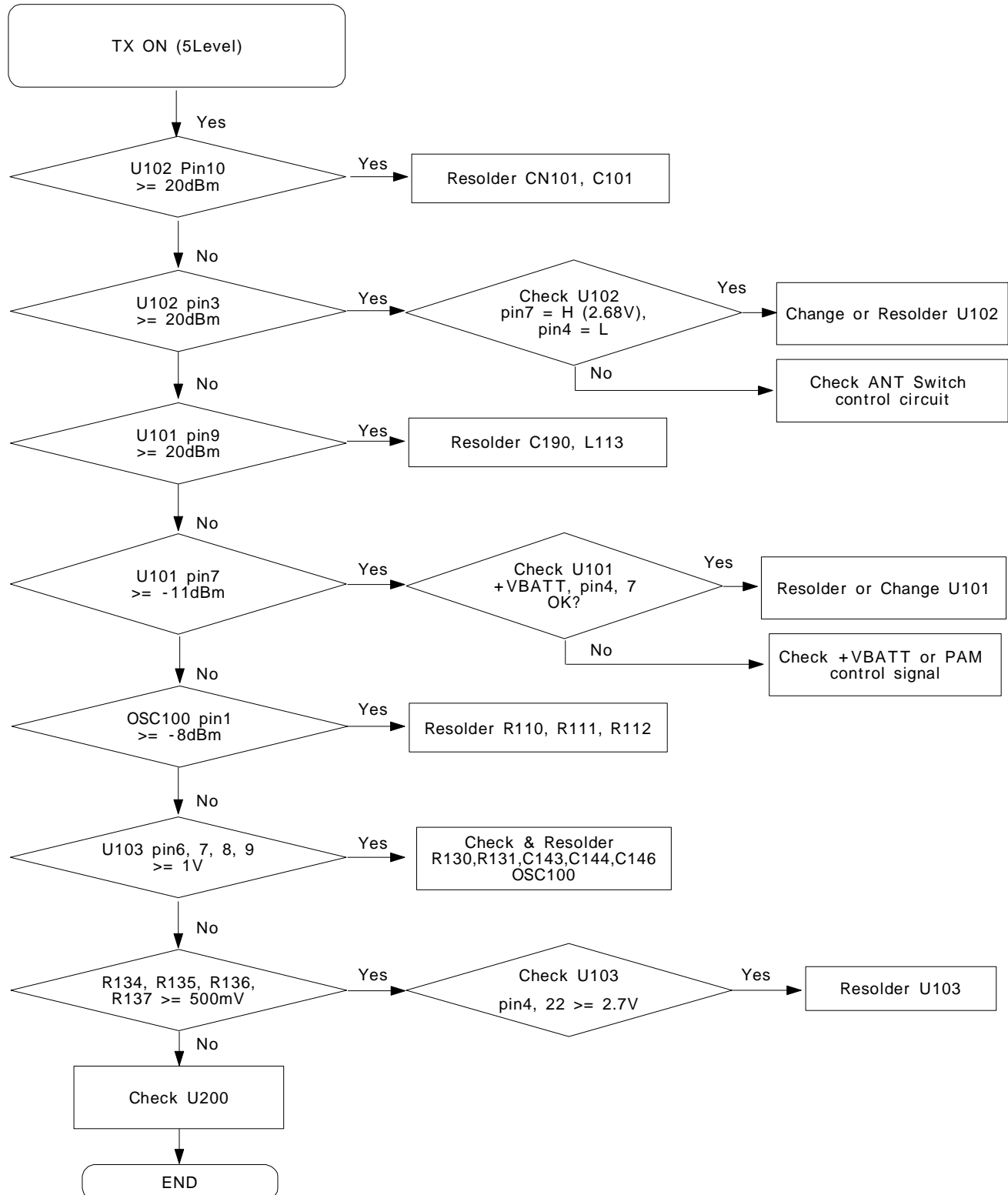
11. Camera part



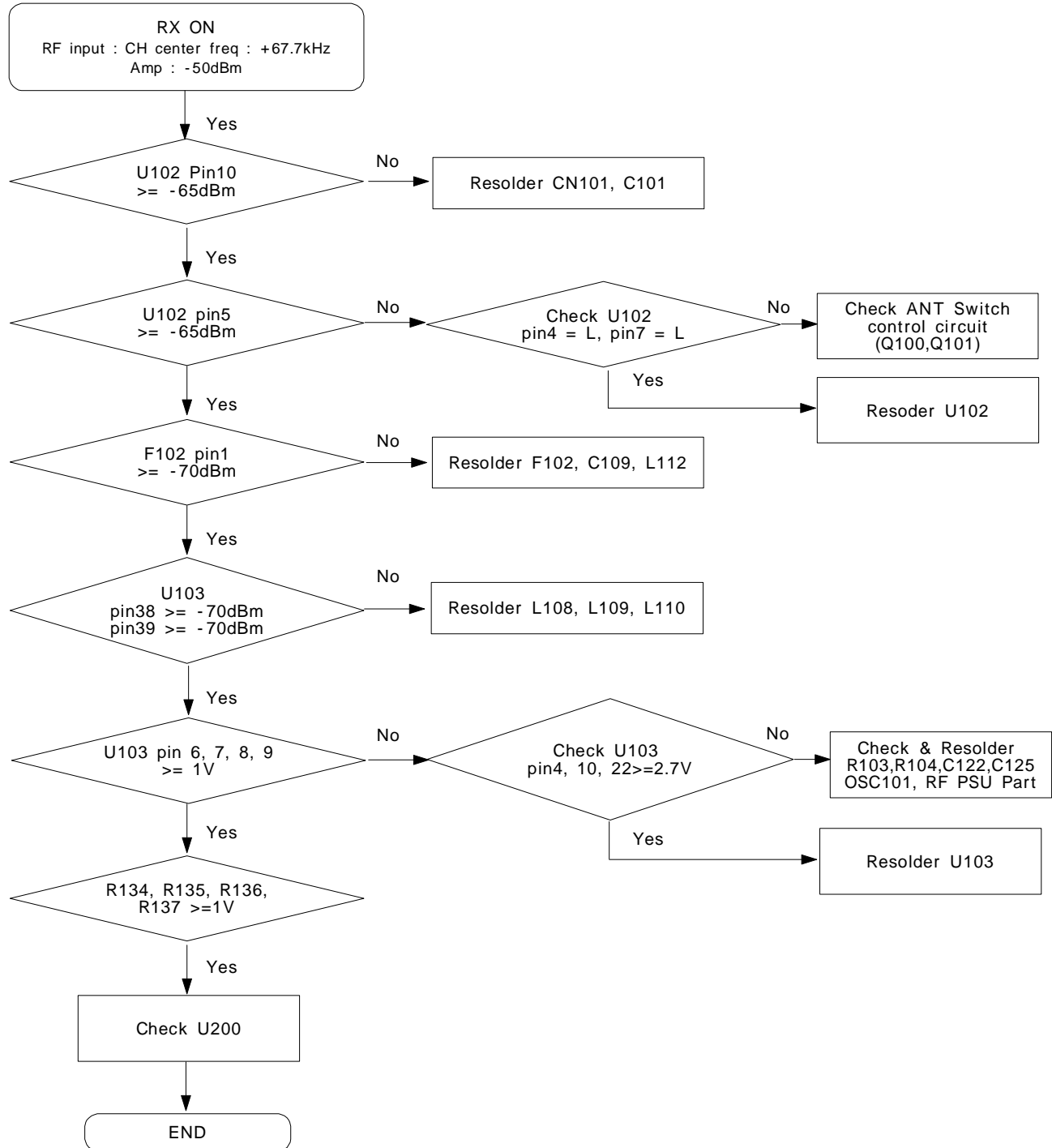
12. GSM Receiver



13. GSM Transmitter



14. DCS Receiver



15. DCS Transmitter

