RX MID CHANNELS
850: CH190 -- 881,6
GSM: CH 62 -- 947,4 MHz
EGSM: CH 37 -- 942,4Mhz
DCS: CH 700 -- 1842,8MHz
PCS: CH 661 -- 1960MHz

PA + Antenna Switch

VRF2
FL102 — TX_HB
FL101 — TX_LB
B+
DCS/PCS OUT
GSM850/ GSM900 OUT
U50 - RAPTOR
Power and Antenna Control
1900 MHZ
1800 MHz
900 MHz
850 MHz

Internal Antenna
M1
(indicates mechanical Antenna connection to U800)
ANT_DETB
J1 Mechanical Antenna Switch

PA Power Control selection via VRAMP, TX_HB and TX_LB
1. IPC: Input Power Control mode - for EDGE mode (PA gain is fixed and PA input power varies)
2.BCM: Bias Control mode - for GMSK mode (PA gain varies according to power step and fixed input PA power)

VDETECT, VRAMP (PA Power Control), TX_EN (Transmit Enable), LB_HB, US_EURO, TX_AUX_SW_EN, IPC_BCM, (Transmit Enable) TX_STARTB, RESETB

GSM / EDGE Tranceiver IC

FL100 Quard Saw Filter and Matching: High Band 1900MHz, High Band 1800MHz, Low Band 900MHz, Low Band 850MHz

U100 -TRANSAAM
PA Control, GPIO, LPF, Digital Radio Receiver, RX CP, RX VCO, TX VCO, TX CP, Phase Modulation, Amplitude Modulation, Transmit Modulator, RX / TX In / Out - Putcontroller, Synthesizer RX / TX Clock, Serial Interface, ADC Voltage Reg.

RXTXEN, RXTXDATA, LEG_SPI_READY, SYSCLKEN, SYSCLK, BT_CLK, BT_CLK_EN, Y101 26MHz, CTRLDATA, CTRLCLK, CTRLEN, VRF1, VRF2, VRFCP, VRFDIG (VCC's from Atlas)

SCMA11 U800

(1.3V, 399/156MHz 1.55V, 532/208MHz) VCORE, VDIG_1.8V, (2,8V) VRFDIG, (2,8V) VIOHI, (1,775V) VRFCP, (3,2V) EFUSE_PGM, (from Atlas) VMMC1, (to Atlas) VMMC_EN, (from Atlas) BAT_DETB, (Reset) SIM_RST, (Clock) SIM_CLK, (Data In /OUT) SIM_IO

Power, SIM Interface, Memory 16KB 32KB, SC140 156MHz turbo 208MHz, Memory 16KB 16KB 128KB, AMR1 399MHz turbo 532MHz, Digital RF Control Interface, Clock Interface, Digital BB Interface, SPI, Keypad Interface, UART / USB Interface, MQSPI, Timer Interface, I2C BUS, One Wire Bus, 1st Serial Audio Port Interface, 2nd Serial Audio Port Interface

(to Atlas) AD_TRIG
(13 MHz) BB_SYS_CLK
(from Atlas) 32K_CLK

133MHz

External Memory Interface, Bluetooth Interface, IPU Interface (Display), Camera Interface, SD Memory Interface, GPIO

DDR DATA D0-15
DATA BUS D0-15
ADDRESS BUS A0-23

U700 FLASH 128MB NAND ROM 64MB SDRAM
DDR_CLK, DDR_CAS_B, DDR_RAS_B, DDR_SDWE_B, DDR_CS3B, DDR_SDCKE, DQM0, DQM1, DDR_SDBA0, DDR_SDBA1, NAND_CS_B, NAND_RE_B, NAND_WE_B, NAND_WP_B, NAND_ALE, NAND_CLE, NAND_R_B, SDCLK_B, MA10, DQS0, DQS1
VDIG_1.8V (from Atlas), VSDRAM (from Atlas)

BT_RTS_B, BT_CTS_B, BT_RX_AP_TX, BT_TX_AP_RX, BT_RESET_B, BT_WAKE_B, BT_HOST_WAKE_B (from/to Bluetooth module U300)

IPU_LD(15:0), IPU_D1CS_LD16, IPU_D0_VSYNC_LD17, IPU_D3_HSYNC, IPU_D3_VSYNC, IPU_D3_DRDY, IPU_D3_CLK, SER_EN, GPIO_DISP_SD (from/to Serializer U650)
IPU_SD_MISO, IPU_SD_MOSI, IPU_SD_CLK (from/to J650 /Flip)

GPIO_DISP_RST_B, GPIO_CLI_SER_RS, IPU_SD_DI_CS, IPU_2D_CS_B, CSI_D(7:0), CSI_MCLK, CSI_VSYNC, CSI_HSYNC, CSI_PIXCLK, GPIO_CAM_RST_B, GPIO_CAM_PD, CLI_ID (from/to J650 /Flip)

SD1_CLK, SD1_CMD, SD1_DATA 0-3 (from/toTransFlash)
MMC_CLK, MMC_CMD, MMC_DATA0 (from/to SIM)

VDIG_1.8V, Hall Sens. U902, VIOHI
FLIP_DET, EL_EN2 (to U901), LOWBAT_B (to U900), POWER_RDY (AMR), POWER_RDY (DSP) (to U900), VVIB_EN (to U900), VFUSE_SEL (to U940), TOUCH_INTB (from J650)

Keyboard Matrix 0-9,*,#,5-Way Navigation — KPP_COL(5:0), KPP_ROW(4:0) — FL771, FL770
Side Keys — KPP_COL(2,4,5), KPP_ROW(3,4)

USB_VPIN, USB_VMIN, USB_VPOUT, USB_VMOUT, USB_RXRD, USB_TXEN_B, USB_XCVR_EN (from/to U900 USB Com.)
BB_SPI_CLK, BB_SPI_MOSI, BB_SPI_MISO, PM_SPI_CS, PM_INTB (SCMA11/Atlas Communication)
BB_STANDBY (from Atlas), RESETB, WDOG_AP, WDOG_BP (to Atlas), LVS (AVS)
I2C_CLK, I2C_DAT (2 wire Serial Bus, 1.8V, Slaves)
BATT_DAT (OneWire data from BATTery)
ASAP_CLK (clock), ASAP_FS (frame sync), ASAP_RX, ASAP_TX (from/to U900)
MMSAP_CLK (clock), MMSAP_FS (frame sync), MMSAP_RX, MMSAP_TX (from/to U900)

Revision Overview
Rev. 1.0: Initial Block Diagram

Servive, Engineering & Optimization	2007.08.10
LEVEL 3 AL Block Diagram	Rev. 1.0
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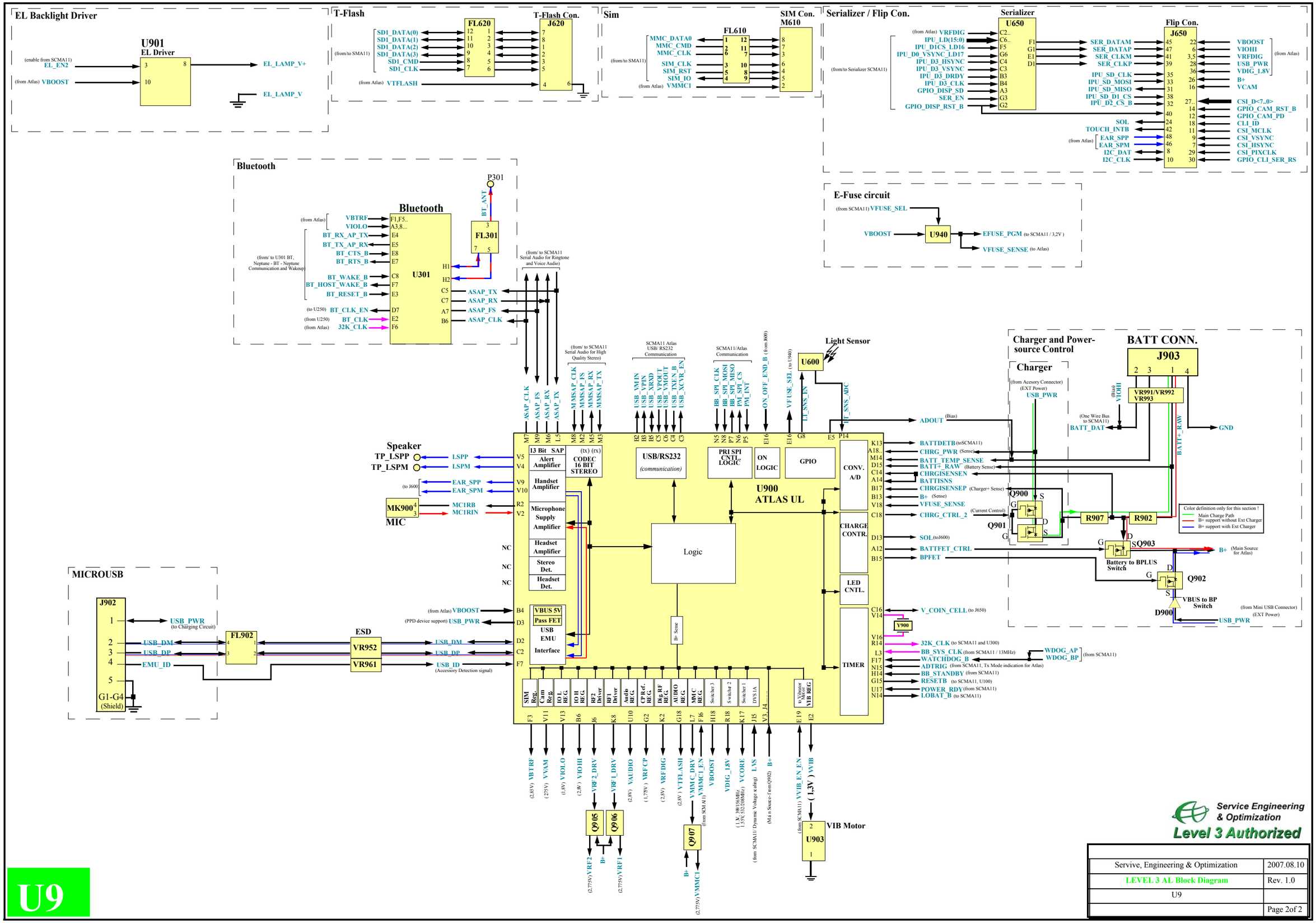
Service Engineering & Optimization
Level 3 Authorized


EL Backlight Driver
U901
EL Driver
EL_EN2
VBOOST
EL_LAMP_V+
EL_LAMP_V
T-Flash
FL620
T-Flash Con.
J620
SD1_DATA(0)
SD1_DATA(1)
SD1_DATA(2)
SD1_DATA(3)
SD1_CMD
SD1_CLK
VTFLASH
Sim
FL610
SIM Con.
M610
MMC_DATA0
MMC_CMD
MMC_CLK
SIM_CLK
SIM_RST
SIM_IO
VMMC1
Serializer / Flip Con.
Serializer
U650
Flip Con.
J650
VRFDIG
IPU_LD(15:0)
IPU_D1CS_LD16
IPU_D0_VSYNC_LD17
IPU_D3_HSYNC
IPU_D3_VSYNC
IPU_D3_DRDY
IPU_D3_CLK
GPIO_DISP_SD
SER_EN
GPIO_DISP_RST_B
SER_DATAM
SER_DATAP
SER_CLKM
SER_CLKP
IPU_SD_CLK
IPU_SD_MOSI
IPU_SD_MISO
IPU_SD_D1_CS
IPU_D2_CS_B
SOL
TOUCH_INTB
EAR_SPP
EAR_SPM
I2C_DAT
I2C_CLK
VBOOST
VIOHI
VRFDIG
USB_PWR
VDIG_1.8V
B+
VCAM
CSI_D<7..0>
GPIO_CAM_RST_B
GPIO_CAM_PD
CLI_ID
CSI_MCLK
CSI_VSYNC
CSI_HSYNC
CSI_PIXCLK
GPIO_CLI_SER_RS
Bluetooth
P301
BT_ANT
FL301
Bluetooth
U301
VBTRF
VIOLO
BT_RX_AP_TX
BT_TX_AP_RX
BT_CTS_B
BT_RTS_B
BT_WAKE_B
BT_HOST_WAKE_B
BT_RESET_B
BT_CLK_EN
BT_CLK
32K_CLK
ASAP_TX
ASAP_RX
ASAP_FS
ASAP_CLK
E-Fuse circuit
VFUSE_SEL
U940
EFUSE_PGM
VFUSE_SENSE
Light Sensor
U600
Charger and Power-source Control
Charger
USB_PWR
BATT CONN.
J903
VR991/VR992
VR993
BATT_DAT
GND
BATT+_RAW
ADOUT
BATTDETB
CHRG_PWR
BATT_TEMP_SENSE
BATT+_RAW
CHRGISENSEN
BATTISNS
CHRGISENSEP
B+
VFUSE_SENSE
CHRG_CTRL_2
SOL
BATTFET_CTRL
BPFET
V_COIN_CELL
32K_CLK
BB_SYS_CLK
WATCHDOG_B
ADTRIG
BB_STANDBY
RESETB
POWER_RDY
LOBAT_B
WDOG_AP
WDOG_BP
Q900
Q901
R907
R902
Q903
Q902
D900
Battery to BPLUS Switch
VBUS to BP Switch
Color definition only for this section !
Main Charge Path
B+ support without Ext Charger
B+ support with Ext Charger
Speaker
TP_LSPP
TP_LSPM
LSPP
LSPM
EAR_SPP
EAR_SPM
MK900
MIC
MC1RB
MC1RIN
U900
ATLAS UL
13 Bit SAP
Alert Amplifier
Handset Amplifier
Microphone Supply Amplifier
Headset Amplifier
Stereo Det.
Headset Det.
CODEC 16 BIT STEREO
USB/RS232
(communication)
PRI SPI CNTL LOGIC
ON LOGIC
GPIO
CONV. A/D
CHARGE CONTR.
LED CNTL.
TIMER
Logic
VBUS 5V
Pass FET
USB EMU Interface
MICROUSB
J902
USB_PWR
USB_DM
USB_DP
EMU_ID
FL902
ESD
VR952
VR961
USB_ID
Q905
Q906
Q907
U903
VIB Motor
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